A suspended-membrane balanced frequency doubler to 200 GHz

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A Suspended-Membrane Balanced Frequency Doubler to 200 GHz

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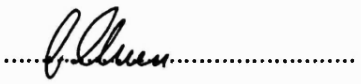

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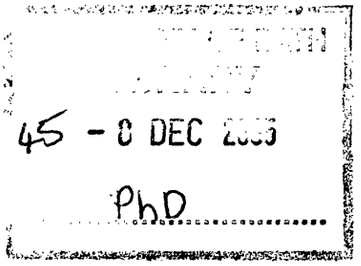
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CHAPTER INDEX

SYMBOL INDEX

Chapter 1

v_p = peak electron velocity
E_T = threshold electric field
v_v = valley velocity
P_e = plasma electron density
f_p = plasma absorption frequency

Chapter 2

Q = charge
V_B = reverse bias
t = time
V = voltage
a_0, a_1.. = constants
V_d = voltage amplitude
ω_g = generator angular frequency
ω = angular frequency
V_g = generator voltage
P_g = generator power
f_g = generator frequency
Z_g = source impedance
Z_l = load impedance
P_n = power at nth harmonic
nf_g = nth harmonic of generated frequency
I_g = generated current
Z_0 = characteristic transmission line impedance
l = length of transmission line
β = phase constant
Y_0 = characteristic transmission line admittance
X_L = inductive reactance
B_c = capacitive susceptance
Z_H = high impedance
Z_L = low impedance
W = microstrip width
d = substrate thickness
ε_r = relative permitivity
Z_m = nominal microstrip impedance
L = inductance
C = capacitance
λ_c = cut off wavelength
$V(z)$ = transmission line voltage
$I(z)$ = transmission line current
j = imaginary number
Z_{in} = line impedance looking at load
R_P = parasitic resistance
C_P = parasitic capacitance
L_B = backshort inductance
R_B = backshort resistance
λ_g = guided wavelength
f = frequency
n = mode index
m = mode index
μ = permeability
ε = permitivity
P_{in} = input power
P_{out} = output power
L = conversion loss
L_n = loss at nth harmonic
nf_{gmin} = lower bandwidth limit
nf_{gmax} = upper bandwidth limit
B = bandwidth
L_{nmax} = maximum insertion loss at the nth harmonic
L_{nmin} = minimum insertion loss at the nth harmonic
Φ_b = barrier potential
V_b = breakdown voltage
R_s = series resistance
V_j = voltage across junction
Q_B = charge at breakdown
q_Φ = charge at barrier/ contact potential
N = harmonic number
R_i = input impedance
R_L = optimised load impedance
D = optimised drive level
Q_{max} = maximum junction charge
γ = junction grading
α = optimizing variable
β_1 = optimizing variable
S_{max} = maximum elastance
C_{min} = capacitance at breakdown
V_{0norm} = normalised bias voltage
G = efficiency
P_L = output power load
V_{dc} = DC bias voltage

Chapter 4

q = charge
Φ_b = barrier potential
Φ_m = metal work function
Φ_s = semiconductor work function
E_{Fm} = Fermi energy level in metal
E_{Fs} = Fermi energy level in semiconductor
E_V = valence band energy level
E_C = conduction band energy level
χ_s = electron affinity
V_n = difference between E_C and E_{Fm}
E_0 = zero energy level
V_d = diffusion (or built-in) voltage
V_b = bias level
w = depletion region width
ε_s = total permitivity
N_D = n layer doping density
V_T = electron transition level ($=kT/q$)
Q_{sc} = charge per unit area
C_j = junction capacitance
A_0 = anode area
R_0 = anode radius
b, b_1, b_2 = constants
γ_c = correction factor
J_b = current density across barrier
A^{**} = modified Richardson constant
J_s = saturation current density
h = planks constant
m^* = effective mass of holes
m_0 = free electron mass
m_r = relative electron mass
ρ = resistivity
r_c = specific contact resistance
R_c = contact resistance
R_{sh} = sheet resistance
W = width of ohmic contact
d = length of ohmic contact
L_t = transfer length
i_d = displacement current in diode
C_j = junction capacitance
i_e = current through undepleted epilayer
n_e = electron density
v_e = electron velocity
$i_{e,max}$ = maximum current through undepleted epilayer
$v_{e,max}$ = maximum electron velocity
μ = drift velocity
E = electric field strength
η = ideality
I_0 = saturation current
R_j = junction resistance
R_1 = undepleted epilayer resistance
L_u = undepleted epilayer inductance
C_u = undepleted epilayer capacitance
t_e = total epilayer thickness
μ_{e0} = epilayer mobility
ρ_e = epilayer resistivity
$\omega_{s,eff}$ = effective scattering frequency
R_2 = spreading resistance
δ = skin depth
ω = angular frequency
μ = electron mobility
σ = conductivity
ρ_n^+ = resistivity of n^+ layer
SF = scaling factor
ϕ = radial overlap of anode in cathode
ϕ_a = angle anode makes with GaAs surface
R_3 = bulk n^+ skin resistance
r_x = distance from centre of anode to edge of cathode
R_4 = resistance through n^+ material into ohmic contact
r_e = distance from centre of anode to edge of diode chip
ρ_n = resistivity of n layer material
C_P = anode layer to n/n^+ layer capacitance
C_F = finger capacitance
C_A = fringing capacitance outside of chip
C_{PP} = internal fringing capacitance
C_1 = anode cone capacitance
C_3 = anode to ohmic capacitance
r = uppermost anode surface radius
r_0 = lowest anode surface radius
r_1 = depletion region capacitance radius
r_2 = anode overhang radius
L_e = length of finger that overhangs active GaAs
t_{ox} = oxide layer thickness

Chapter 5

L_{eff} = effective backshort position
L = backshort length

WP = probe width
D = probe depth
WI = inductor width
LI = inductor length
WC = cavity width
WD = width of 50 Ω line
G = microstrip to waveguide top
HC = cavity height
HD = substrate thickness
ε_r = relative permitivity
λ_g = guided wavelength
E_{max} = maximum E field strength
C = backshort variable
k_1, k_2 = scaling constants
μ = permeability
ε = permitivity
ω = angular frequency
d = scaling dimension
σ = conductivity
c = speed of light
f_c = cut-off frequency
m, n = mode indices
a = waveguide width
b = waveguide height
I = current
V = voltage
Z_{emb} = embedding impedance
V_s = source voltage
Z_s = source impedance
R_L = load impedance
$\overset{+}{V}$ = polarised voltage source
$\underset{-}{}$
a_n (n = 1, 2, 3...) = constant
I_L = load current
f_n = frequency of n^{th} harmonic
Z_g = gap source impedance
h_g = height of gap source above substrate
A_g = gap source area
h_m = membrane height in guide

Chapter 6
V_s = source voltage
Z_s = source impedance
Z_L = load impedance
R_j = diode nonlinear resistance
C_j = diode nonlinear capacitance
C_1 = parasitic capacitive element 1
C_2 = parasitic capacitive element 2
V_B = DC bias voltage
Z_B = DC bias source impedance
$i(t)$ = current waveform
$V(t)$ = voltage waveform
l = length of transmission line
λ_0 = free space wavelength
N = positive integer
L_{eff} = effective backshort position
N_D = epilayer doping concentration
R_s = diode series resistance

Chapter 7
η = diode ideality factor
R_s = diode series resistance
t_m = thickness of metal deposited
A_r = diode anode diameter
R_{oc} = ohmic contact resistance
V_{br} = diode breakdown voltage
C_j = diode junction capacitance
V_b = bias applied to diode
A_0 = anode area
N_D = epilayer doping concentration
V_{bi} = diode built-in voltage

Chapter 8
A_r = diode anode diameter
t_e = total epilayer thickness
N_D = epilayer doping concentration
Φ_b = barrier potential
η = diode ideality factor
R_s = diode series resistance
V_{br} = diode breakdown voltage
C_{j0} = zero bias junction capacitance
C_p = diode parasitic capacitance

Chapter 9
R_s = diode series resistance
N_D = epilayer doping concentration
Φ_b = barrier potential
C_p = diode parasitic capacitance
L_{eff} = effective backshort position

Chapter 1

Introduction

The principle driving force behind this work is the need for continuous wave power from a solid state device of the order of several hundred gigahertz for use in heterodyne instrumentation. As these frequencies cannot be generated directly at the power level required, lower frequency signals are multiplied up by successful implementation of, predominantly, frequency doublers or triplers.

1.1 Heterodyne Receiver

Frequency multipliers are used as an essential link in the many parts that constitute heterodyne receivers. A schematic diagram of a submillimetre receiver is shown in Fig. 1.1.

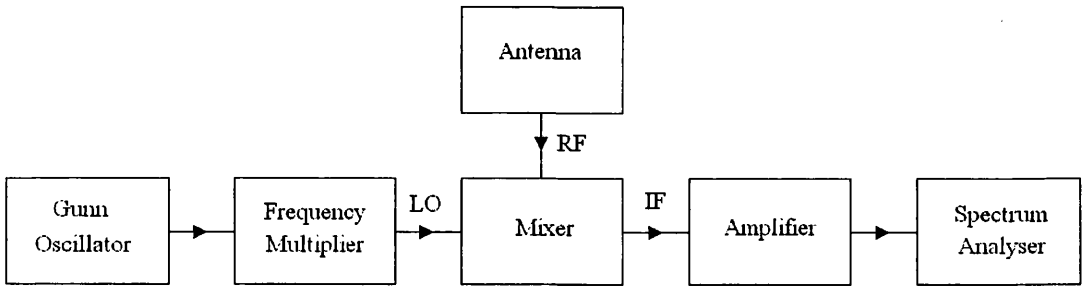


Fig. 1.1 Schematic layout of a submillimetrw receiver.

The input or radio frequency (RF) signal is sent to the input of a mixer via the antenna or telescope. Also input to the mixer is a local oscillator (LO) signal which is generated by a source (Klystron or more commonly Gunn oscillator) and multiplied up in frequency. Inside the mixer the LO and RF signal are electrically mixed, converting the RF information to the lower intermediate frequency (IF). Assuming sufficient power the IF signal is amplified and detected. In order for the receiver to work correctly the LO signal, which has to be generated, needs to be close in frequency to the RF (to within a few GHz). The LO device nominally used in these systems is the Gunn diode which is limited to a maximum frequency output of

around 200GHz, (much higher frequencies have been attained but at very low power levels) but more typically used around 100 GHz. Therefore for receiver systems requiring detection above 100 GHz frequency multipliers must be implemented.

1.2 Elements of the Receiver

1.2.1 Mixer

When the RF and LO signals have been combined and sent to the mixer a nonlinear element generates the sum and the difference frequencies. The difference or IF frequency is of the most importance. The IF signal, which is usually of the order of a few gigahertz, is easily filtered from the rest of the output signal and then amplified before detection which is generally more sensitive and less noisy than direct detection. The heterodyne mixer system also has the invaluable advantage of being tuneable over a broad bandwidth. Changing the LO source frequency can be achieved by tuning the LO backshort allowing the mixer to detect a large range of frequencies.

1.2.1.1 Superconductor Insulator Superconductor (SIS) Mixer

Two superconducting contacts separated by a ~20 Å insulator forms the nonlinear element of the SIS mixer. The most sensitive receivers use SIS mixer technology for mm and sub-mm wavelengths. These devices are limited to frequencies where the incoming photon energy exceeds that of the energy gap of the superconducting material. Above these frequencies, 700 GHz for niobium, the mixer performance drops as the device becomes very lossy. Superconducting compounds such as NbN [1.1] and TiNbN [1.2] have been investigated where this effective frequency limit has been pushed to 1.2 THz. The SIS mixer is usually the first choice for astronomical observations due to its high sensitivity and need for highly cooled components.

1.2.1.2 GaAs Schottky Diode Mixer

GaAs Schottky diode mixers are generally less sensitive than SIS mixers. The development of GaAs Schottky mixers, however, still compromises a large amount of work. Pioneering work in the 1960's brought about the whisker contacted GaAs

Schottky diode chip. The whisker contact, a thin pointed wire gives the device minimal parasitic capacitance which is one of the main contributors to power loss in modern devices. The thin wire also has unwanted inductive properties that can be reduced by changing the whisker shape and length. However the difficulty in mounting and general mechanical instability of whisker contacted diodes opened the door for a new approach. The integrated planar GaAs Schottky diode overcomes the instability and fabrication difficulties inherent with whisker contacts.

The technology for GaAs Schottky diode mixers is well established and can easily reach THz frequencies. Performance limitations arise from the inherent parasitic losses and large LO power requirements. Schottky diode mixers operate at room temperature but much more efficiently at cryogenic temperatures, displaying less noise. Schottky diode mixer based receivers are usually selected for space applications because of their ability to operate at a variety of temperatures and their mechanical stability.

1.2.2 LO Power Source

In the region of 250 GHz to 10 THz useable solid state sources do not exist. Above this band optical devices such as lasers and LED's can be implemented. Some researchers have achieved high frequency sources around 600 – 700 GHz but at power levels not sufficient to operate most mixers. Some optical mixers, [1.3, 1.4] which combine high frequency (~THz) optical signals and extract the difference frequency can be used as terahertz power sources. Again, optically generated power sources simply cannot deliver the necessary power levels to drive most mixers.

1.2.2.1 Gunn Diodes

Gunn diodes are the standard choice for most mm-wave LO sources. Fundamental to the operation of the Gunn diode oscillator is the Negative Differential Region (NDR) in their I/V characteristics. Fig. 1.2 shows the electron drift velocity as a function of applied electric field. As an electric field is applied the drift velocity increases linearly until it reaches the peak velocity, v_p, at the threshold electric field, E_T. Beyond E_T there is a region of negative differential mobility and then the mobility levels out at the valley velocity. This behaviour is due to a unique band structure that appears in some semiconductors, present in GaAs, and is shown in Fig. 1.3. At low

electric fields electrons occupy the bottom of the central valley. As the electric field strength is increased the electrons in the central valley occupy a broader range of energies until their kinetic energy exceeds 0.36 eV. When this happens the electrons have the opportunity to transfer to one of the satellite valleys that lie along the <100> crystallographic directions, see Fig. 1.3. The effective mass of the electrons in the satellite valleys is approximately six times that of the central valley and the mobility is approximately 70 times less, [1.5].

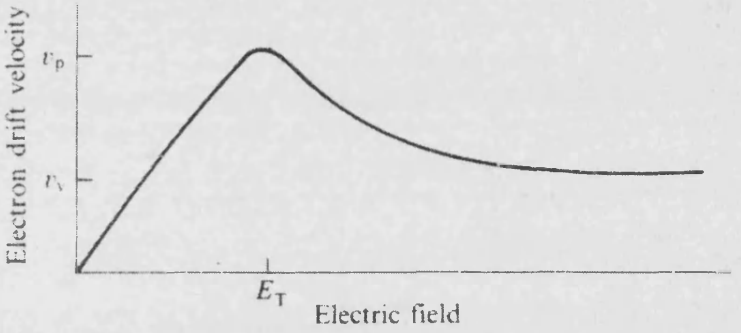


Fig. 1.2 Electron velocity as a function of applied electric field. The peak electron velocity, v_p, arises at the threshold electric field denoted by E_T and v_v is the valley velocity (see later), [1.5].

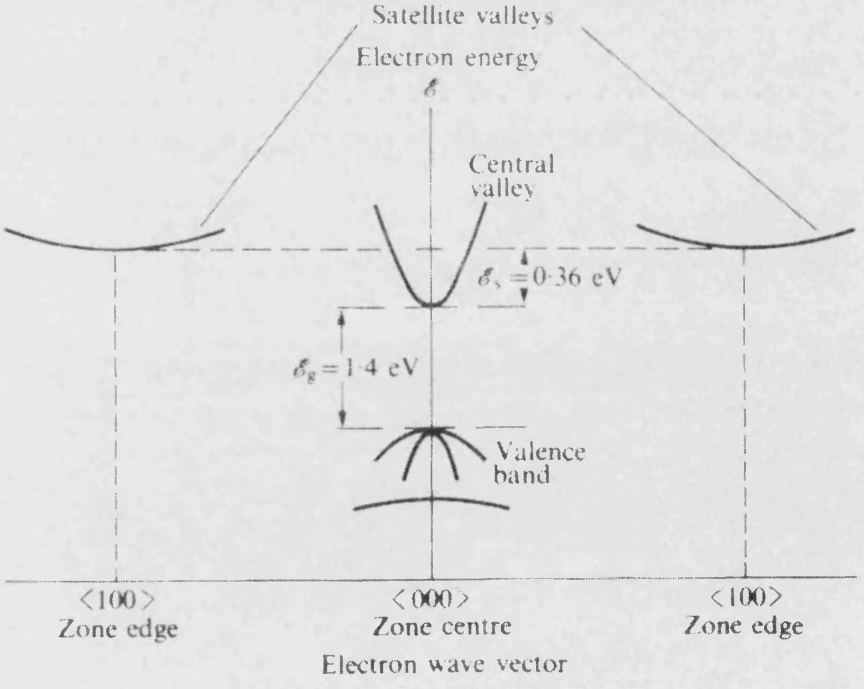


Fig. 1.3 Band structure in GaAs, [1.5].

The Gunn diode is made of a small section of this semiconducting material with two contacts on either side, the anode and cathode. On application of an electric field above E_T, the carriers will pass from the cathode and accelerate through the material to velocity v_p. After peaking at v_p the carriers enter the negative differential region on entering the lower mobility satellite bands. The carriers then drift at the valley velocity, v_v, set by the valley mobility out of the material via the anode. Overall, the effect is a fluctuation in electron density across the semiconductor, i.e. a resonant pulsing. The length of the semiconductor and the shape of the terminals along with the doping density all contribute to the response of the diode. The limitation to the frequency response of a Gunn diode, determined by the transit time from the central to satellite valley, is usually of the order of 100 GHz.

High performance InP Gunn devices have yielded high output powers and frequencies up to 300 GHz. State of the art Gunn diodes have been fabricated using $n^+/n/n^+$ structures with graded doping profiles. Effective heat sinking has dramatically improved operating characteristics in InP Gunn devices resulting in RF powers exceeding 200 mW at 103 GHz [1.6]. Power combining pushes this figure to something nearer 300 mW at 106 GHz. Operation in second harmonic mode, by tuning of the output circuit, has power over 3.5 mW at 214 GHz.

1.2.2.2 Transistors and Other Devices

High electron mobility transistors (HEMT) have also been used as solid state sources. They have been demonstrated to produce powers around 60 mW at 94 GHz and high efficiency, [1.7]. Recent developments also suggest they could potentially be used to generate terahertz frequencies but are limited to how small the components can be fabricated.

Other devices such as heterojunction bipolar transistors (HBT's) and field effect transistors (FET's) have also been used to generate signals of the order of one to two hundred gigahertz. The operation cut-off frequency for HBT's is lower than that of FET devices but reducing the distance between the ohmic contact and base connection can give significant increases. Because of the vertical structure type of the HBT a multiple array of finger contacts could be implemented to increase power handling of the devices.

1.3 Applications

A description of a child's toy, a primitive radio receiver from the 1920s, is given by Hines in 1984 [1.8]. The receiver was a small box containing no vacuum tubes and required no power source. The box had two external tuning knobs, a binding post and a *crystal*. After connection of an aerial, ground wire and ear phones, the user probed the polycrystalline multifaceted surface of the galena crystal, held in a metal cap, with a pointed spring wire known as a 'cat whisker'. After finding a sensitive spot the local radio station could be heard.

This is an early record of a solid state electronic device and at least 20 years ahead of the transistor. Two other papers from Thomas in 1909 [1.9] and Hunt and Whittmore in 1916 [1.10] were among the first reports that RF detection can occur between metals and non-metallic crystal materials. For completeness, the first reference of the directional behaviour of current through the metal/ non-metallic crystal interface can be found in a paper by Ferdinand Braun in 1847 [1.11].

Southworth [1.12] was exploring the propagation of ultra high frequency (UHF) radio waves during his time at Bell laboratories during the 1930's. He was able to find sources of UHF and microwave energy and could transmit these signals down transmission lines and waveguides. However, there was still no satisfactory detection method. The vacuum tube and triode tube could not respond to these high frequencies and this resulted in the resurrection of the crystal rectifier. Two of Southworth's colleges, King and Ohl, later devised a more stable and reliable detector. A sharp metal point held against a polished surface of silicon, not too dissimilar to the child's toy described by Hines. To quote Southworth, "It was Mr Ohl who first triggered the chain reaction that not only led not only to the modern microwave rectifier, but the solar battery, the transistor and finally the broader field now generally know as solid state physics." And finally to quote Hines, "There is no doubt in my mind that the crystal rectifier was, and remains, the most important, the most indispensable and perhaps the least appreciated of microwave devices." Apart from advances in materials and fabrication techniques the concept is very much the same today. The modern Schottky barrier junction used in microwave detectors today differs very little from Ohl's crystal rectifier.

1.3.1 Radio Astronomy

The submillimetre wavelength spectral band, covering the frequency range 0.1 – 10 THz, represents one of the least explored yet information rich segments of the EM spectrum. This frequency span encompasses all of the critical spectral emissions from the key molecules involved in atmospheric chemistry on earth, studies of the early stages of star formation in interstellar molecular clouds [1.13, 1.14] and for observations of the cosmic background radiation, [1.15]. Several submillimetre telescopes are in operation today such as the James Clerk Maxwell Telescope (JCMT) [1.16] and the Caltech Submillimeter Observatory in Hawaii, along with those under construction, e.g. the Submillimeter Array of the Smithsonian Astrophysical Observatory. There are several space missions planned by ESA and NASA to carry heterodyne receivers for detection of submillimetre wavelength radiation through astronomical observations, e.g. HERSCHEL launching early 2007 will be observing the formation of galaxies and stars and the chemical composition of the Earth's atmosphere, PLANK launching with HERSHEL will map the Cosmic Microwave Background with improved sensitivity and test inflationary models of the early universe

For these observations to operate correctly the detection equipment must have very low noise and maximum sensitivity usually giving rise to cryogenically cooled detectors. High spectral resolution is also needed for molecular line astronomy. Submillimetre wave spectroscopy can be used to study spectral lines occurring due to rotational transitions of simple non-symmetric molecules such as ^{12}CO, ^{13}CO, HCO^+, CN and others found in interstellar medium. These molecules are generally sparse and found only in trace quantities embedded in interstellar clouds of hydrogen. Analysis of the spectral line structure can be used to determine temperature, density and motions of the material making up the molecular cloud.

Diffuse molecular clouds collapse under their self-gravitational attraction. Protostars can be formed by the formation of clumps of material from within the molecular clouds as a result of its gravitational instability. Cosmic rays and UV radiation cause ionization of these atoms and molecules which leads to some complicated chemistry. Of key importance is the astronomical observation of carbon, neutral carbon (CI) and

molecular carbon (CO), which is thought to provide the critical cooling mechanism during the collapse of dust clouds into stars, [1.15]

Much attention has been given to the study of neutral carbon in molecular clouds. The $^3P_1$ -> $^3P_0$ transition of CI at 492 GHz has been widely observed throughout molecular clouds and external galaxies, [1.13].

The JCMT is the world's largest facility designed specifically to make observations in the submillimetre region of the spectrum. At an altitude of 4092 m, near the summit of Maunakea, Hawaii, it is above 97 % of the water held in the atmosphere. The facility operates instruments in four frequency bands, A (215 – 275 GHz), B (318 – 373 GHz), C (430 – 510 GHz) and D (630 – 710 GHz). Most of the heterodyne observations are concerned with the early stages of star formation, including formation rate, planets not yet formed from dust disks and extragalactic observations.

SOFIA, the Stratospheric Observatory For Infrared Astronomy is a NASA operated Boing 747 mounted high altitude (44'000 feet) telescope commencing Summer 2005. SOFIA observations will include: chemical compositon of galxies, early stages of star formation, composition and structure of planetery atmospheres, interstellar clouds and Ultra-Luminous IR Galaxies (ULIRGS) as a key component in the early stages of the creation of the universe. CASMIR, Caltech Submillimeter and Far-Infrared Mixing Receiver, is the heterodyne receiver for SOFIA. This project will look at a number of problems (astrophysical) including the evolution of galaxies and to the birth and death of stars. SIS mixers working with frequencies up to 1200 GHz will be used in this project.

1.3.2 Atmospheric Remote Sensing

Microwave remote sensing developed in the 1960's [1.17, 1.18] along with technology advances to higher frequencies has opened up the possibility of atmospheric sensing. Submillimetre and millimetre wavelength heterodyne spectroscopy from orbiting satellites is a technique used to monitor the Earth's upper troposphere, stratosphere, mesosphere and lower thermosphere. NASA's Upper Atmosphere Research Satellite (UARS) was one such experiment utilising this

technique. Covering frequency bands near 63, 183 and 205 GHz and having primary targets ClO, O_3, H_2O and measurements of temperature and pressure, the experiment delivered important information on the chemistry of the Earth's atmosphere. Measurements of ClO are important for understanding and monitoring the chlorine depletion of ozone. A secondary instrument will determine H_2O_2 and HNO_3 concentrations and wind velocity in the mesosphere.

European Space Agency (ESA) remote sensing projects using submillimtre receivers MASTER, using a 1 m diameter antenna covering frequency bands up to 500 GHz, and SOPRANO, using a 2.2 m diameter antenna covering frequency bands up to 950 GHz, will observe various atmospheric species including H_2O, O_3, HNO_3, ClO, BrO.

1.3.3 Chemical and Biological Warfare Agent Detection

The threat of attack in either warfare or terrorist situation may call for the use of reliable chemical and biological (CB) agent detectors. An adequate defence would necessitate the ability to rapidly detect and identify both known and unknown threat agents. Woolard has shown that due to a large number of unique resonant features that arise from phonon modes, the terahertz regime can be extremely useful for the study, analysis and identification of biological macromolecules under controlled laboratory conditions, [1.19]. Fig. 1.2 shows a block layout of a ground- or air-based active sensor looking at a cloud of dry bioparticles.

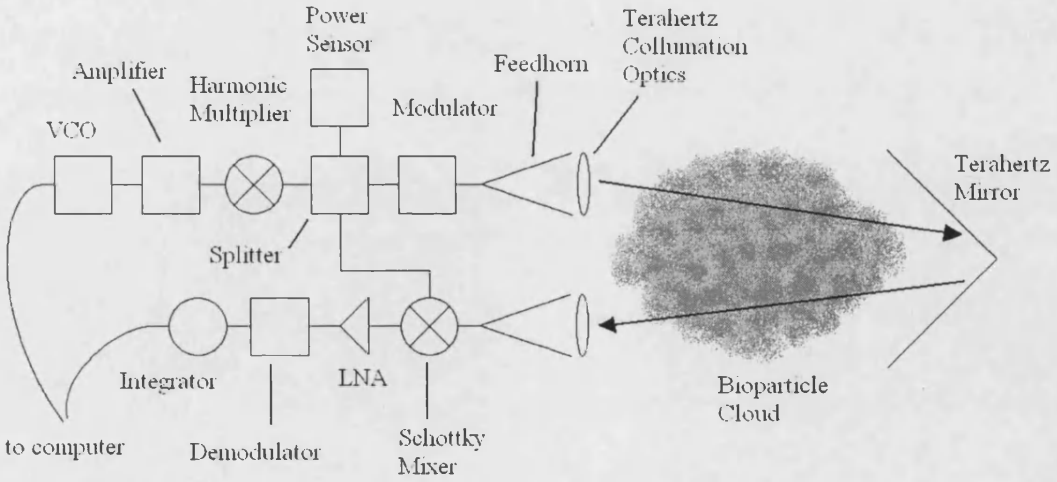


Fig. 1.2 Schematic diagram of potential bioparticle cloud detector [1.19].

Studies on DNA [1.20] and complete biological samples revealed detailed and high level numerical structures. This is possibly due to vibrational lattice and local phonon modes and other physical mechanisms of interactions between radiation and biological materials. This technique for detection involves THz-frequency spectroscopy utilising a Differential Absorption Radar which detects the spectral signatures of Bacillus Subtillus spores. Absorption signatures of the B. Subtillus range from 327 GHz to 1075.5 GHz.

1.3.4 Communication Systems

Stimulated in part by the availability of new microwave technology, demand is growing rapidly worldwide for wideband telecommunications. Archer [1.21] and Batchelor [1.22] at CSIRO Division of Radiophysics, Australia, are at the leading edge of the technology involved in this area. Millimetre-wave gallium arsenide Monolithic Microwave Integrated Circuits (MMIC's) are a key component of the broadband and high data rate wireless local-area networks that are being investigated. The high absorption effect of the atmosphere and narrow beam widths make these wavelengths well suited to intra-building, secure, high speed, wireless communication links. A 40 GHz communication system is available from Microwave Networks Australia and development of a 60 GHz 100 Mbit s^{-1} is underway at CSIRO.

Shoji *et al* [1.23] have developed a self-heterodyne broadband signal transmission system at the Communications Research Laboratory, Kunugawa, Japan. The mm-wave remote self-heterodyne transmission system enables extremely stable and low cost broadband transmission at 60 GHz. Fig. 3 gives a pictorial suggestion of how such a system may be used. An incoming satellite broadcast signal is sent to the millimetre transmitter via a satellite receiver which is then sent to other millimetre-wave receivers throughout the house, e.g. television, video or laptop computer. The transmitter of the system delivers RF modulated signals and an LO signal simultaneously and the signal is received through a square-law-type detection technique. This creates a very stable and low phase-noise mm-wave transmission link without the need of advanced frequency stabilisation technology. Without the need of an LO source the devices can be miniaturized and the cost reduced. The

team demonstrated the transmission of a modulated satellite broadcast video signal with 300 MHz bandwidth over a distance of 8m.

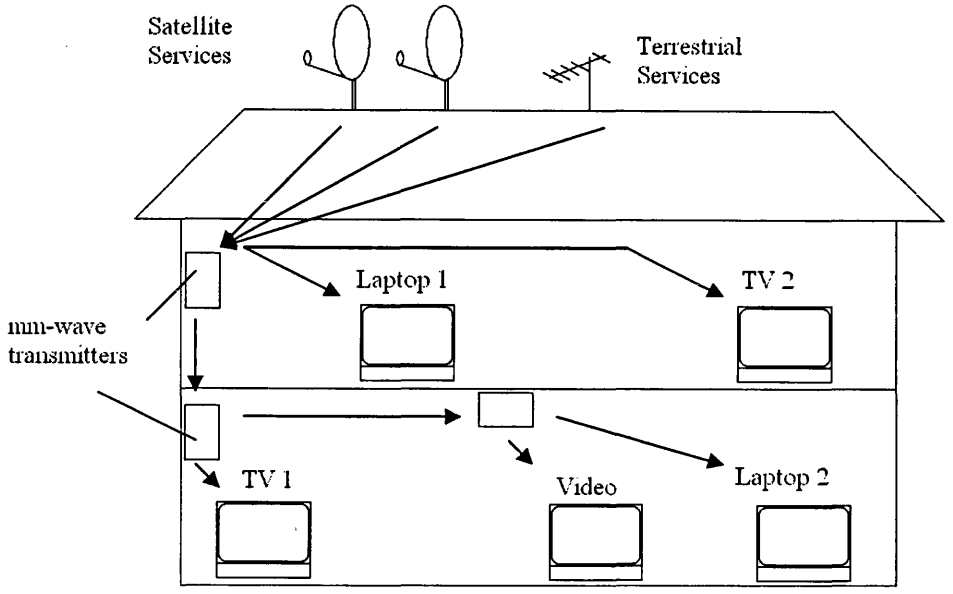


Fig. 3 Millimeter wave video transmission system, [1.23].

1.3.5 Plasma Diagnostics

Many properties can be deduced by looking at the absorption, scattering and phase shift of mm-wave radiation through plasma, [1.24, 1.25]. The plasmas electron density (P_e) and temperature can be found through absorption of a certain frequency (f_p) given by

$$f_p = 8.974\sqrt{P_e}\,. \tag{1.1}$$

Electron density at 10^5 electrons cm^{-3} pushes f_p into the sub-mm range and hence diagnostic tools are required to cover this range [1.26].

1.3.6 Explosives and Weapon Detection

Concealed weapons and explosives have always been of concern to public safety in places such as airports. The terrorist attacks on New York in September 2001 and the bombing of Pan Am flight 103 indicated the need of more sophisticated systems. Despite the success of portal metal detectors, based on eddy current distortions of magnetic fields, there remains no reliable non-invasive detection of other potentially

harmful weapons. Weapons such as plastic or ceramic knives and explosives can be concealed under clothing and undetectable in these conventional approaches.
At mm-wavelengths most clothing material has a very low absorption factor and hence appears 'see-through'. To be able to detect a concealed object such as a gun or a knife, the object of concern must have a higher or lower reflection coefficient compared to that of the background, i.e. human body, resulting in a reflectivity contrast. The higher the reflectivity contrast the more 'visible' the object would be after the signal has been processed through advanced imaging software. Also the resolution of the sensor system must be small compared to object size, < 0.1 object length [1.27]. There are two approaches to this concept: real aperture radar and radar holography, [1.28]. Real aperture radar has advantages including: relative simplicity and low cost, available technology, ease of generation, transmission and storage of TV format images and relatively simple signal processing. However resolutions on these systems are generally too low to get clean identification of weapons. In microwave holography, similar in principle to optical holography, the amplitudes and phases of the radiation reflected from the target are used to reconstruct a near perfect images. Researchers, [1.27] have built radar holographic imaging systems operating at 22 to 47.5 GHz, 40 to 60 GHz and 90 to 120 GHz. A UK team [1.28, 1.29] have recently completed trials of a real time mm-wave imager at 33 GHz. Constructed at QinetiQ, Malvern, UK, the trials in both laboratory and a real airport environment resulted in the successful detection of ceramic and plastic weapons. Plastic explosives were more difficult to locate.

The applications for millimetre and submillimetre wave systems are fairly moderate and cover a broad base of areas. In most cases the area is highly specialised and no mass market potential could develop in these areas. The exceptions are the communications and weapon/ explosive detectors. Low cost, reliable, wireless links for computer networks are already commercially available at moderate transfer rates and no doubt these rates will increase over time. Non-invasive security scanning systems are operational in airports and other places where it is inconvenient to manually search people and their luggage. As soon as the processes described above, such as holographic imaging systems, have been refined they should start to be introduced to airports across the world. Ultimately, frequency multipliers have a principle use as an integral part of the highly specialised heterodyne receiver systems.

1.4 Summary

1.4.1 Harmonic Generation

Electronic devices with nonlinear I/V or C/V characteristics have been used for many years to generate higher frequencies from lower frequencies by the process of frequency multiplication. This has been done with vacuum tubes, semiconductor diodes and transistors. The varactor diode, as a low-loss nonlinear reactive element, was quickly recognised to have potential for highly efficient frequency multiplication. When driven with a sinusoidal current at one frequency, its voltage waveform becomes distorted and rich in harmonics without a great loss in energy. With suitable knowledge of the system impedances, input and output matching circuits can be used to restrict a selected harmonic to the output of the multiplier.

1.4.2 Project Originality

Conventionally sub-mm wave frequency multipliers have been fabricated through a process called *flip chip bonding*. This involves the accurate placement and soldering of a tiny semiconductor chip (~100 x 200 um) onto, usually, the contact pads of a quartz substrate containing the rest of the circuit. Soldering, involving high temperatures, is required for the stability of its various applications, i.e. space launches. The high temperatures can cause these tiny electrostatic sensitive devices to fail. Furthermore, the series resistance of the circuit, which is needed to be as low as possible, is generally increased through flip chip bonding.

Integration can be achieved by making the substrate and diode out of the same material, i.e. gallium arsenide. This method eliminates the need of flip chip bonding and allows direct integration with the microstrip transmission line and microstrip filter formation if required. Gallium arsenide has a high dielectric permittivity (~12.9) and hence is very lossy in high frequency circuits. However, by reducing the thickness of the substrate down to a few tens of microns this lossy effect can be minimised and this should be highly beneficial to the efficiency of the multiplier system.

The aim of this work was the design, fabrication and successful testing of a 200 GHz frequency doubler using monolithic integrated membrane diode technology.

References – Chapter 1

[1.1] Y. Uzawa, A. Kawakami, S. Miki and Z. Wang, "Performance of All-NbN quasi-Optical SIS mixers for the Terahertz band," *IEEE Transactions on Applied Superconductivity*, vol. 11, issue. 1, March 2001, pp. 183-186.

[1.2] B. D. Jackson, N. N. Oisad, G. de Lange, A. M. Baryshev, W. M. Laauwen, J.-R. Gao and T. M. Klapwijk, "NbTiN/SiO_2/Al tuning circuits for low-noise 1 THz SIS mixers", *IEEE Trans. on Applied Superconductivity*, vol. 11, no. 1, March 2001, pp. 653-656.

[1.3] Q. Z. Liu, R. I. MacDonald, "Controlled nonlinearity monolithic integrated optoelectronic mixing receiver," *IEEE Photonics Technology Letters*, vol. 5, no. 12, December 1993, pp. 1403- 1406.

[1.4] S. B. Alexander, "Design of wide-band optical heterodyne balanced mixer receivers," *Journal of Lightwave Technology*, vol. LT-5, no. 4, April 1987, pp. 523-537.

[1.5] G. S. Hobson, "The Gunn effect," *Claredon Press*, Oxford, 1974.

[1.6] H. Eisele, *et al.*, "Recent advances in the performance of InP Gunn devices and GaAs TUNNETT diodes for the 100 – 300 GHz frequency range and above," *IEEE Trans. on Microwave Theory and Techniques*, vol. 48, no. 4, April 2000, pp. 626-631.

[1.7] P. M. Smith *et al.*, "W-band high efficiency InP-based power HEMT with 600 GHz f_{max}," *IEEE Microwave and Guided Wave Letters*, vol. 5, no. 7, July 1995, pp. 230-232.

[1.8] M. E. Hines, "The virtues of nonlinearity – detection, frequency conversion, parametric amplification and harmonic generation," *IEEE Trans. on Microwave Theory and Techniques*, vol. MTT-32, no.9, September 1984, pp. 1097-1104.

[1.9] L. W. Thomas, Experience with the crystal type of wireless detector," *Electrical World*, vol. LIV, no.21, November 1909, pp. 1234-1235.

[1.10] V. A. Hunt and L. E. Whittmore, "Some characteristics of crystal detectors," *Science Abstracts*, vol. VXIX-B-1916, pp. 269-271.

[1.11] F. Braun, "On the current conduction through metallic sulfides," *Hittorf. Pogg. Ann.*, vol.84, 1847, pp. 81-85.

[1.12] G.C. Southworth, *Forty Years of Radio Research.* New York: Gordon and Breach, 1962.

[1.13] L. T. Little, *et al.*, "The Cl/CO ratio in the molecular cloud G34.3+0.2," *Monthly Notice of the Royal Astronomical Society*, vol. 271, 1994, pp. 649-661.

[1.14] T. H. Buttgenbach, *et al.*, "Submillimeter detection of extragalactic Cl emission – IC 342," Astrophysical Journal, vol.397, 1992, L15-L17.

[1.15] T. G. Phillips, "Submillimeter astronomy," *Proc. of the IEEE*, vol. 80, no. 11, November 1992, pp. 1662-1678.

[1.16] S. R. Davies, *et al.*, "JCMT receiver A2-a 210-280 GHz SIS receiver," IEE Colloquium on Millimeter and Sub-Millimeter Wave Heterodyne Receivers, 1992, pp. 6/1-4.

[1.17] G. Dobson, *et al.*, "Measurements of the amount of ozone in earths atmosphere and its relation to other geophysical conditions," *Proc. Roy. Soc. London*, vol. A122, 1929, pp. 456-486.

[1.18] J. W. Waters, "Submillimeter-wavelength heterodyne spectroscopy and remote sensing of the upper atmosphere," *Proc. of the IEEE*, vol.80, no.11, November 1992, pp. 1679-1701.

[1.19] D. L. Woolard, *et al.*, "Terahertz-frequency remote-sensing of biological warfare agents," *IEEE MTT-S Digest WE5A-7*, 2003, pp. 763-766.

[1.20] D. L. Woolard, *et al.*, "Submillimeter-wave phonon modes in DNA macromolecules," *Phys. Rev. E*, vol.65, May 2002.

[1.21] J. W. Archer, "Australian millimeter-wave MMIC technology for wideband telecommunications systems," *Proc. on 4th Annual Conf. MM-Wave and Far-Infrared Science and Technology*, 12-15 August 1996, pp. 141-144.

[1.22] R. A. Batchelor, *et al.*, "Australian activities in microwave links for wireless LANs," *Microwave Symposium Digest IEEE MTT-S International*, vol.2, 14-18 June 1993, pp. 677-680.

[1.23] Y. Shoji, *et al.*, "Millimeter-wave remote self-heterodyne system for extremely stable and low cost broad-band signal transmission," *IEEE Trans. on Microwave Theory and Techniques*, vol. 50, no. 6, June 2002, pp. 1458-1468.

[1.24] A. Mardon, "Applications of millimeter waves," M*illimeter and Submillimeter Waves*, Ed. F. A. Benson, Illife Books Ltd., 1969, pp. 525-527.

[1.25] S. Xuemin, "Electron cyclotron absorption measurements in a tokamak plasma using the five channel E-band millimetre-wave system," *Proc. Int. Conf. on Microwave and Millimeter-Wave Technology ICMMT*, 18-20 August, 1998, pp. 623-625.

[1.26] P. Woskoboinikow, "Development of gyrotrons for plasma diagnostics," *Review of Scientific Instruments*, vol. 57, no. 8, pt. 2, August 1986, pp. 2113-2118.

[1.27] R. W. McMillian, *et al.*, "Concealed weapon detection using microwave and millimetre-wave sensors," *Proc. Int. Conf. on Microwave and Millimeter-Wave Technology ICMMT*, 18-20 August, 1998, pp. 1-4.

[1.28] O. Minin, "Quasioptical mm-wave concealed weapon detection systems: review," *Proc. Int. Symp. the 7th Korea-Russian Science and Technology KORUS*, vol. 3, June 28 – July 6, 2003, pp. 60-64.

[1.29] K. J. Murphey, *et al.*, "Millimeter-wave aviation security scanner," *Proc. Int. Conf. 36th Annual Security Technology*, 20-24 October, 2002, pp. 162-166.

Chapter 2

Multiplier Theory

Frequency multipliers operate principally on the strong nonlinearities present in their devices, [2.1]. The nonlinear device is usually a diode and this project was concerned mainly with the gallium arsenide Schottky diode. This type of diode is classified as a varactor, meaning it has a nonlinear relationship between capacitance and voltage as shown in Fig. 2.1. Another type of device used is the varistor diode which exhibits a strong nonlinear current/ voltage characteristic. The varistor is generally less used due to poor conversion efficiency to higher frequencies and hence lower power output.

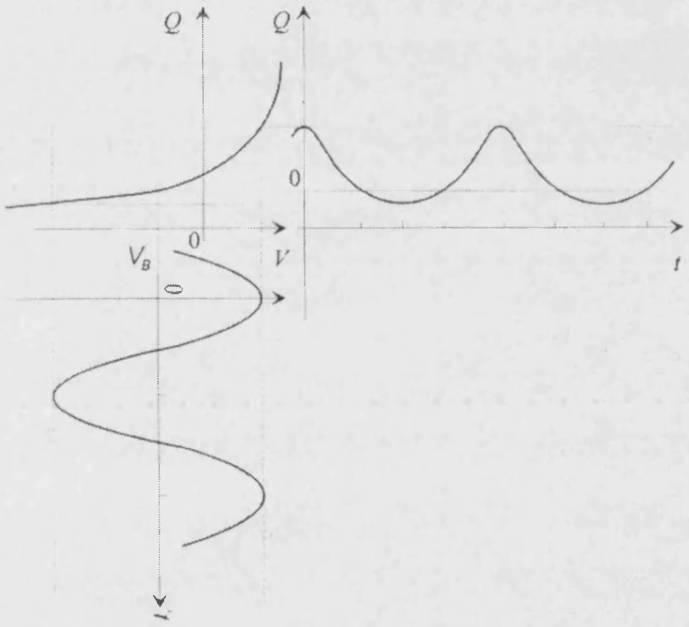


Fig.2.1 *Q/V* response for a varactor with sinusoidal input signal and V_B applied reverse bias [2.2].

2.1 Multiplier Theory

Fig.2.1 shows how the charge of a reversed biased varactor junction can be modulated by addition of a sinusoidal voltage waveform. This results in the periodic time-dependent rectified output signal seen on the RHS of Fig.2.1. The output signal

contains components at harmonic multiples of the input frequency which is the basis of higher order multiplication.

The nonlinear Q/V relationship can be mathematically expanded about its fixed bias voltage using a power series [2.2]

$$Q(V_B + \Delta V) = a_0 + a_1 \Delta V + a_2 \Delta V^2 + a_3 \Delta V^3 + \ldots \tag{2.1}$$

where V_B is the bias voltage across the device. The input voltage applied to the device is given by,

$$\Delta V = V_d \cos(\omega_g t) \tag{2.2}$$

where V_d is the amplitude of the input waveform, ω_g is the angular frequency of the generator and t is time. Substituting the input waveform (2.2) into (2.1) we arrive at the following:

$$Q(V_B + \Delta V) = a_0 + a_1 V_d \cos(\omega_g t) + a_2 V_d \cos(2\omega_g t) + \ldots \tag{2.3a}$$

$$Q(t) = Q_0 + Q_1 \cos(\omega_g t) + Q_2 \cos(2\omega_g t) + \ldots . \tag{2.3b}$$

Equation (2.3b) shows the presence of harmonics generated from the input signal. This approach however may seem to restrict the order of the multiplier to the degree of nonlinearity present in the device, i.e. in order to achieve a third harmonic the device must exhibit characteristics in its power series to a third degree. However this is not the case due to nonlinear element mixing properties. Assume a device which exhibits a square-law C/V relationship, i.e.

$$Q(V) = a_0 + a_1 V + a_2 V^2 . \tag{2.4}$$

Applying the same voltage waveform to the device (2.2), we arrive at the time-dependent charge output waveform, i.e.

$$Q(t) = Q_0 + Q_1 \cos(\omega_g t) + Q_2 \cos(2\omega_g t). \tag{2.5}$$

This can be substituted into (2.4) to get to the next level approximation,

$$Q(t) = Q_0 + Q_1 \cos(\omega_g t) + Q_2 \cos(2\omega_g t) + Q_3 \cos(3\omega_g t). \qquad (2.6)$$

As a result of the fundamental frequency mixing within the third term of (2.5) the third order harmonic appears. In the case of designing a frequency tripler, the filtering and matching networks would need to be designed in such a way that the input signal at the second and third harmonics could exist across the device. In such a case a real part of the circuit impedance at the third harmonic would need to exist with filtering circuits that isolated the third harmonic to the output circuit. This is an example of where idler circuits are used. Here the second harmonic is used in an idler circuit, i.e. currents at this frequency do not pass to the output but their existence is essential to the operation of the multiplier.

2.2 Circuit Considerations

When designing a doubler, however, no idler circuits are used but it is necessary that the circuit should not absorb energy at harmonics higher than the second. Therefore it is necessary to suppress currents at third and fourth harmonics. If this is done effectively then there will be a greater amount of power available at the second harmonic and hence higher available output power. In order to do this, filtering and matching networks are employed as shown in Fig. 2.2. In Fig. 2.2 a source of fundamental frequency generates a signal of voltage V_g which has power P_g, frequency f_g and an internal impedance Z_g. Through design and implementation of filters and matching networks the output across the load, Z_l, will have a power P_n at the chosen n^{th} harmonic frequency nf_g.

Input filters restrict output frequencies to the output circuit, similarly output filters will allow only currents at the output frequency to pass from device to output. Matching circuits in microstrip can be fabricated using tuning stubs [2.3] or radial stubs [2.4]. Backshorts are used for matching in waveguide circuits which can sometimes be adjustable through implementation of a sliding plug.

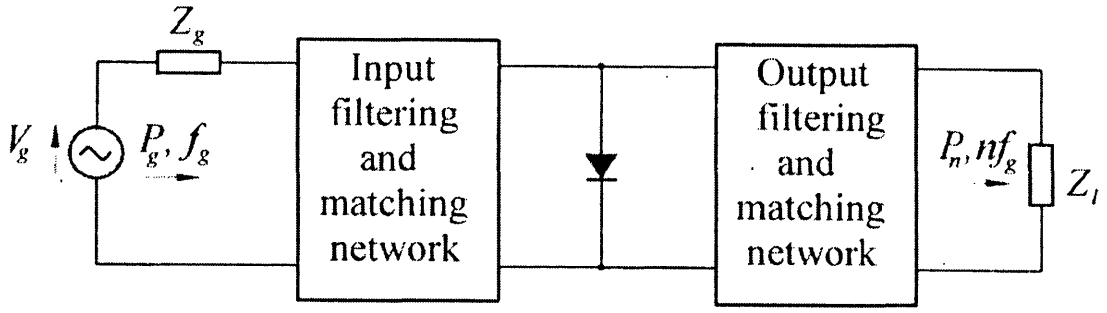


Fig. 2.2 Circuit diagram of a multiplier showing location of input and output matching circuits [2.2].

Balanced circuit topology is a method used to reduce circuit design and fabrication labour. Observed first for mm-wave frequency multipliers in a design by Erickson [2.5], the balanced design eliminates the need of some filters which are lossy to the circuit and improves the power handling of the multiplier. A similar design was implemented by Archer [2.6] where two separate diodes in different waveguides are driven by a single power source and the outputs are combined and put into phase. The Archer design was balanced but the Erickson design has a clear advantage. Having the two diodes in different waveguides meant that the diodes could not be combined on a single chip, greatly increasing construction complexity.

Two main configurations exist for balanced multipliers. A schematic circuit design for an anti-series configuration is shown in Fig. 2.3a and an anti-parallel configuration is shown in Fig. 2.3b. Two diodes in an anti-parallel configuration result in even harmonics confined to the immediate device loop and as a result are suppressed in the output circuit. Two diodes in an anti-series configuration results in the suppression of odd harmonics generated in the output circuit. The suppressed currents in either case can be thought of as being in a *virtual loop*, [2.7]. This is quite obviously a great advantage when considering the design of a doubler or tripler. The anti-parallel diode configuration employed in a frequency tripler serves as a 'natural' filter for even harmonics eliminating the need for a filter between input and output circuits at the output frequency. Similarly, a balanced doubler with anti-series diode configuration will suppress odd harmonics resulting in more available power at the output frequency.

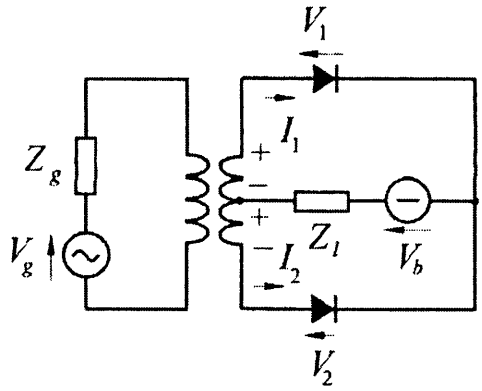


Fig. 2.3a Frequency multiplier with anti-series diode configuration. Voltage V_1 is dropped across diode in upper loop due to current I_1 and similarly voltage V_2 is dropped across diode in lower loop due to current I_2. Both loops share a common load and both diodes are biased identically, [2.2].

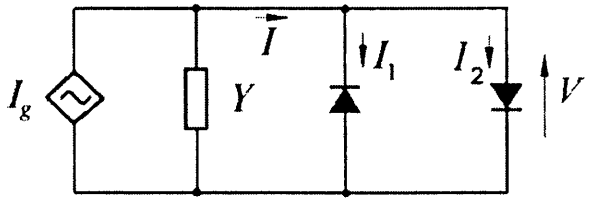


Fig. 2.3b Frequency multiplier with anti-parallel diode configuration. A current source provides a current I_g to the anti-parallel diode circuit which has an admittance Y. Current will only flow through one of the diodes during each half of the AC applied signal at any single moment in time, [2.2].

The multiplier in this project used two varactor diodes in a balanced anti-series configuration. For the purpose of this project and the methodology used in acquiring the simulated results, the equivalent circuit needed to be simplified to account for just one diode. This was possible due to electrical symmetry in the transmission lines. This simplified the circuit model to that seen in Fig. 2.4 and allowed the use of existing harmonic balance software. The diode embedding impedance is the impedance of the entire circuit seen between the contact terminals of the diode, A and B in Fig. 2.4. It was crucial to calculate this quantity as accurately as possible in order for the proceeding steps of the design and the results to be reliable.

Nearly half of this project was concerned with the modelling of the circuit in Fig. 2.4 and can be split into two main categories: diode characterising and embedding impedance modelling. Chapter 4 covers the varactor diode modelling and the components of impedance that need to be considered. Chapter 5 includes a detailed

discussion of the embedding impedance using a sophisticated Finite Element Analysis (FEA) program. The next two sections of this chapter deal with the DC isolation filter and input/ output waveguide backshorts, also crucial for the successful operation of the multiplier. All three of these components were then used in the final stage of modelling, the harmonic balance analysis where the information from Chapters 2, 4 and 5 were combined to give predictions of multiplier output power and efficiency.

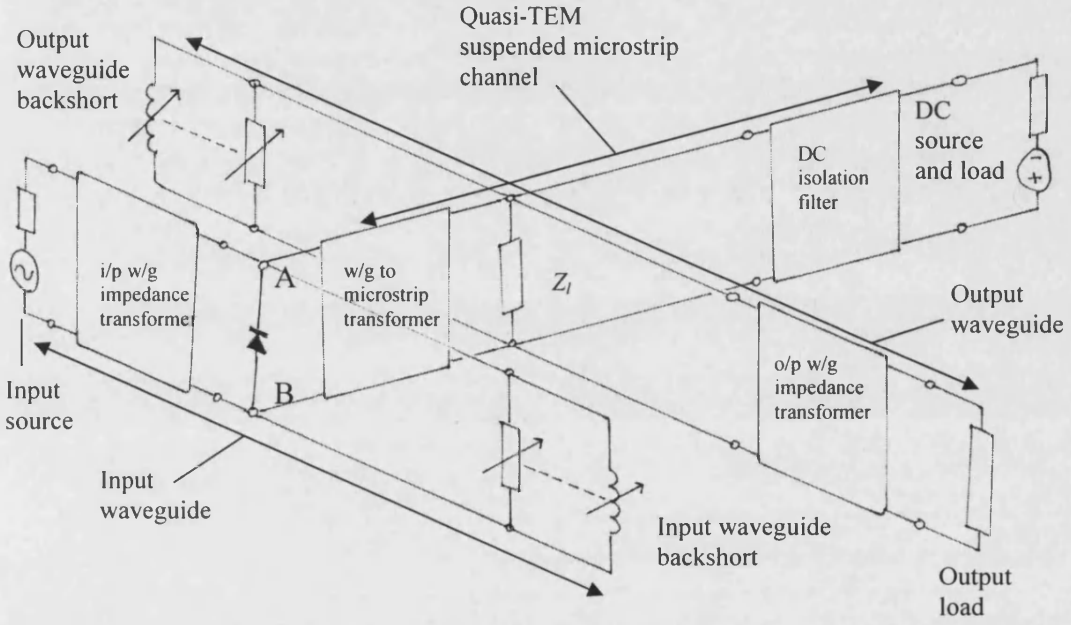


Fig. 2.4 Shows a simplified representation of the proposed circuit where a single diode replaces the anti series connected diodes for simplicity. Input and output waveguides run parallel joined by a quasi-TEM suspended microstrip channel, that continues between Z_l to the DC source.

2.3 Filter Theory and Design

Isolation of high frequency currents inside a multiplier may not always be possible through use of a virtual loop. In these cases stepped-impedance microstrip filters can be used. These filters are used almost exclusively when isolating high frequency currents from an external DC source in frequency multipliers and mixers. Microstrip low pass filters provide an unbroken low resistance electrical path for the DC used to bias the devices. The study and design of these filters is well documented, [2.8], and this section will cover the design procedure for a balanced 200 GHz doubler.

The chosen design for the 200 GHz balanced frequency doubler needed only one microstrip filter for isolating the output RF signal from the DC source. The diodes were in an anti-series configuration and therefore a virtual loop was created at odd harmonics requiring no filtering at these frequencies. Since the second harmonic was generated in the input waveguide it was important to ensure no power at this frequency coupled into the input waveguide and was lost as a result. According to Porterfield [2.9] the lowest order mode that can couple to the input guide is the TM_{11}. This mode can be cut off by reducing the height of the input guide sufficiently. This is demonstrated in Chapter 5.

To summarise, the input signal at 100 GHz coupled into the diodes generating harmonics. Odd harmonics were confined to the immediate circuit in a virtual loop and required no further attention. The second harmonic is not supported by the input guide because the waveguide height is sufficiently reduced. Therefore the final consideration is the RF isolation of the DC terminal which is covered below.

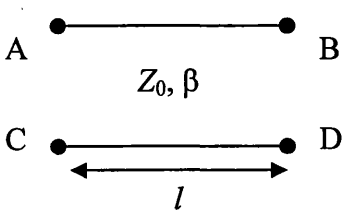
2.3.1 Filter Theory

Because of their ease of fabrication and design a stepped impedance, or hi-Z, low-Z, filter was chosen for the DC isolation. Since the pass-band for these filters was essentially DC there were no requirements for sharp cut-off responses. Stepped impedance filters can be designed to have high insertion loss (> 30 dB) and can be made with relative ease using standard semiconductor fabrication processes.

The stepped impedance filter is a two port network constructed of alternating high and low impedance sections of transmission line. We can approximate these sections of transmission lines to an equivalent circuit of characteristic impedance Z_0. From [2.10] the 2-port ABCD parameters of a length, l, of transmission line are given by

$$A = \cos\beta l \qquad B = jZ_0 \sin\beta l$$

$$C = jY_0 \sin\beta l \qquad D = \cos\beta l$$



where the phase constant $\beta = 2\pi/\lambda$ and the conversion to Z-parameters are as follows,

$$Z_{11} = Z_{22} = \frac{A}{C} = -jZ_0 \cot \beta l \tag{2.7a}$$

and

$$Z_{12} = Z_{21} = \frac{AD - BC}{C} = -jZ_0 \csc \beta l. \tag{2.7b}$$

This results in a series element given by

$$Z_{11} - Z_{12} = jZ_0 \tan\left(\frac{\beta l}{2}\right) \tag{2.8}$$

and the shunt element is Z_{12}. If $\beta l < \pi/2$ series elements are positive and therefore inductive and the shunt elements are negative and therefore capacitive. In this situation the equivalent circuit is represented by Fig. 2.5 where

$$\frac{X}{2} = Z_0 \tan\left(\frac{\beta l}{2}\right) \tag{2.9a}$$

$$B = \frac{1}{Z_0} \sin \beta l. \tag{2.9b}$$

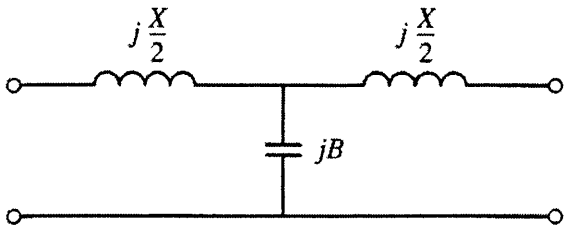


Fig 2.5 Equivalent circuit of the short transmission line for section having $\beta l < \pi/2$, [2.10].

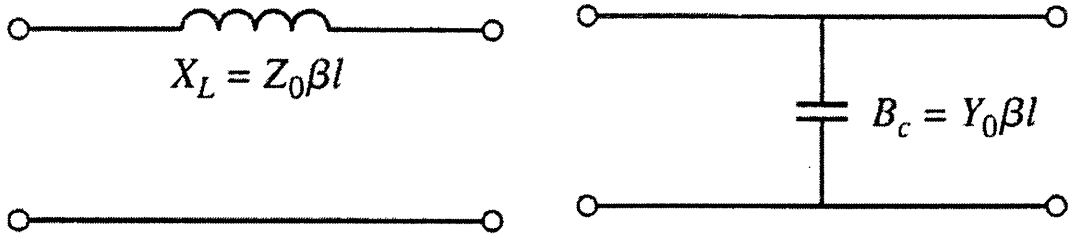
Now if a short length of transmission line is examined with $\beta l < \pi/4$ and a high impedance then (2.9) is approximated as

$$\begin{aligned} X &\approx Z_0 \beta l \\ B &\approx 0 \end{aligned} \tag{2.10}$$

and the equivalent circuit is a series inductor as shown in Fig. 2.6a. A similar length with a low characteristic impedance is approximated as

$$X \approx 0$$
$$B \approx Y_0 \beta l \tag{2.11}$$

and the equivalent circuit is shown in Fig. 2.6b, now a shunt capacitor.



(a) (b)

Fig. 2.6 Equivalent circuit of a small section of transmission line with a small βl and (a) large Z_0 (b) small Z_0, [2.10].

Therefore the inductive and capacitive sections of the transmission line can be generated by using high impedance, Z_H, and low impedance, Z_L, line sections respectively. Fabrication and/ or design limitations will ultimately determine the highest and lowest impedances possible. The filter used in this project was based on sections of microstrip transmission line. The limits to Z_L and Z_H were therefore determined by the width of the microstrip cavity and the limits of the UV lithography (with which the filter pattern was made) respectively. The width of the cavity was chosen to be 0.3 mm ensuring no parasitic modes other than the quasi-TEM can propagate; see Chapter 4 for a demonstration. This sets the upper limit of the microstrip width to be 0.22 mm and a semi-arbitrary lower limit of 0.01 mm was chosen.

Z_H and Z_L can be calculated from the geometry of the microstrip line. The microstrip transmission line is simply a lithographically printed conductor of width W on a substrate with thickness d and relative permittivity ε_r which sits on an earthed plane as shown in Fig. 2.7.

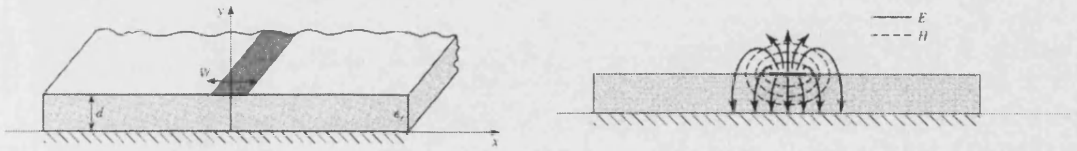


Fig. 2.7 Cut-through section of a microstrip transmission line and the corresponding E and H field lines, [2.10].

Because the E and H field lines travel in two types of material with two different relative permittivities, the phase velocity is different either side of the boundary. For this reason the microstrip cannot support a pure TEM wave and the exact field lines are a hybrid between TM and TE and is termed quasi-TEM.

Because of this hybrid status the impedance of the line is calculated using an effective dielectric constant. This accounts for some of the field lines travelling in the substrate and some in air. The effective dielectric constant is given by [2.10]

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12d/W}}. \tag{2.12}$$

The microstrip impedance is therefore determined by the width of the line, substrate thickness and effective dielectric constant given by

$$Z_0 = \frac{60}{\sqrt{\varepsilon_e}} \ln\left(\frac{8d}{W} + \frac{W}{4d}\right) \qquad \text{for W/d} \leq 1 \quad (2.13a)$$

$$Z_0 = \frac{120\pi}{\sqrt{\varepsilon_e}\left[W/d + 1.393 + 0.667 \ln(W/d + 1.444)\right]} \qquad \text{for W/d} \geq 1. \quad (2.13b)$$

The length of each transmission line can now be found by scaling (2.10) and (2.11) in both frequency and impedance using [2.10]

$$L' = \frac{Z_m L}{\omega}$$
$$C' = \frac{C}{Z_m \omega} \tag{2.14}$$

to

$$\beta l = \frac{LZ_m}{Z_H} \tag{2.15}$$

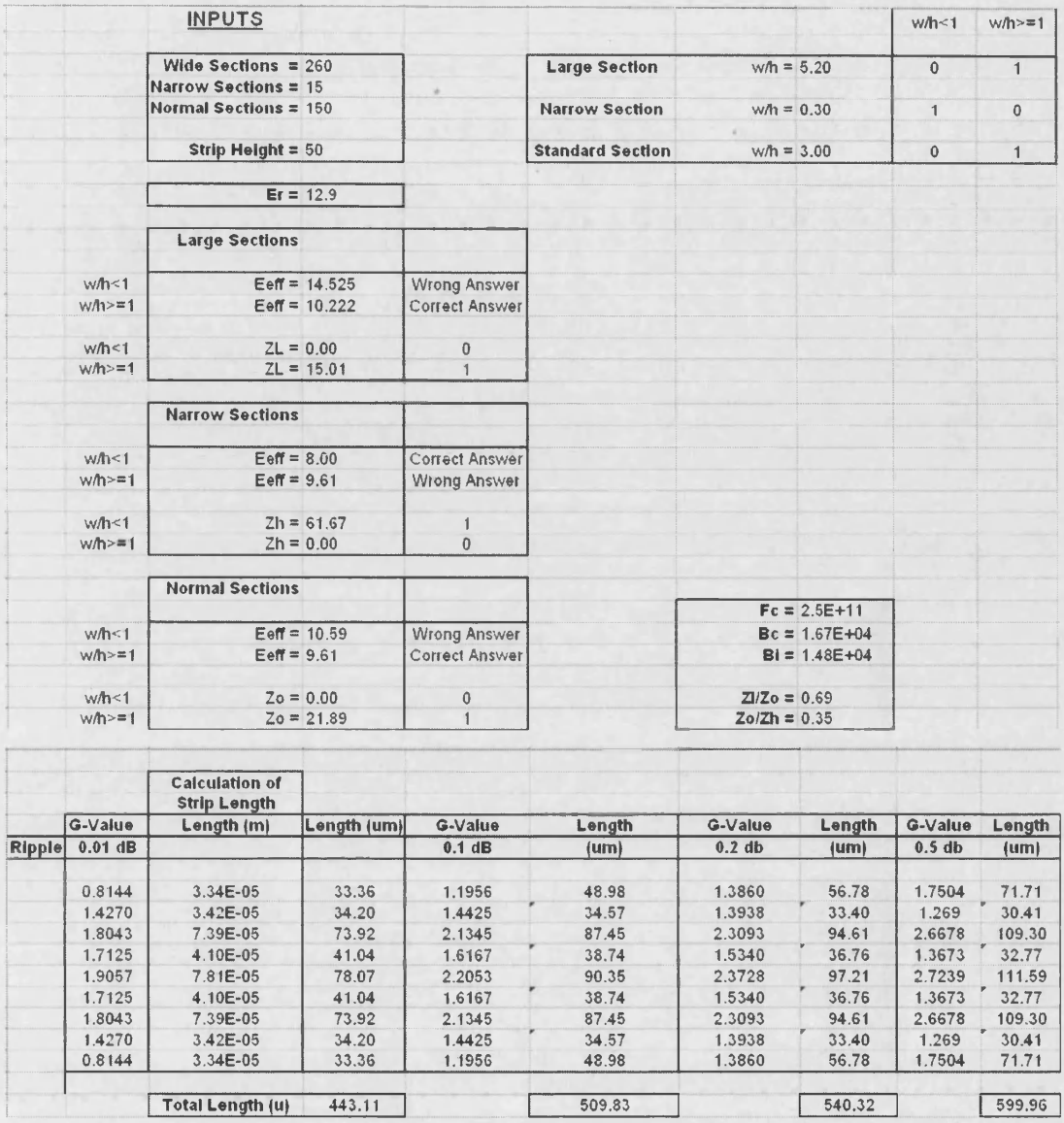
for an inductive element and

$$\beta l = \frac{CZ_L}{Z_m} \tag{2.16}$$

for a capacitive element where Z_m is the impedance of the microstrip line on either side of the filter and $\beta = 2\pi / \lambda_c$ where λ_c is the cut off wavelength. Finally the number of elements to the filter must be determined. More filter elements result in a sharper filter response with a greater insertion loss although restrictions on space may be an issue. Element values can then be assigned to each microstrip section. Odd elements will be capacitive and even elements will be inductive. These element values, or *G-values*, can be found in sources such as [2.8] and can be used to calculate *l* for each section of the filter.

2.3.2 Filter Design

The designing of the filter can be somewhat of a time-consuming task when calculating each element length manually. A simple spreadsheet, shown in Fig.2.8, was implemented to quickly calculate the element lengths for various element widths, dielectric values and cut off frequencies. The spreadsheet also included different pass-band ripple values which determine the structure in the filters pass-band. Since the pass-band for this filter is DC there is no need for any specific pass-band structure and the ripple effect can be exploited to give greater insertion loss at the desired frequencies.



INPUTS					w/h<1	w/h>=1
Wide Sections = 260 Narrow Sections = 15 Normal Sections = 150			Large Section	w/h = 5.20	0	1
			Narrow Section	w/h = 0.30	1	0
Strip Height = 50			Standard Section	w/h = 3.00	0	1
Er = 12.9						

Large Sections		
w/h<1	Eeff = 14.525	Wrong Answer
w/h>=1	Eeff = 10.222	Correct Answer
w/h<1	ZL = 0.00	0
w/h>=1	ZL = 15.01	1

Narrow Sections		
w/h<1	Eeff = 8.00	Correct Answer
w/h>=1	Eeff = 9.61	Wrong Answer
w/h<1	Zh = 61.67	1
w/h>=1	Zh = 0.00	0

Normal Sections		
w/h<1	Eeff = 10.59	Wrong Answer
w/h>=1	Eeff = 9.61	Correct Answer
w/h<1	Zo = 0.00	0
w/h>=1	Zo = 21.89	1

Fc =	2.5E+11
Bc =	1.67E+04
Bl =	1.48E+04
Zl/Zo =	0.69
Zo/Zh =	0.35

		Calculation of Strip Length							
	G-Value	Length (m)	Length (um)	G-Value	Length	G-Value	Length	G-Value	Length
Ripple	0.01 dB			0.1 dB	(um)	0.2 db	(um)	0.5 db	(um)
	0.8144	3.34E-05	33.36	1.1956	48.98	1.3860	56.78	1.7504	71.71
	1.4270	3.42E-05	34.20	1.4425	34.57	1.3938	33.40	1.269	30.41
	1.8043	7.39E-05	73.92	2.1345	87.45	2.3093	94.61	2.6678	109.30
	1.7125	4.10E-05	41.04	1.6167	38.74	1.5340	36.76	1.3673	32.77
	1.9057	7.81E-05	78.07	2.2053	90.35	2.3728	97.21	2.7239	111.59
	1.7125	4.10E-05	41.04	1.6167	38.74	1.5340	36.76	1.3673	32.77
	1.8043	7.39E-05	73.92	2.1345	87.45	2.3093	94.61	2.6678	109.30
	1.4270	3.42E-05	34.20	1.4425	34.57	1.3938	33.40	1.269	30.41
	0.8144	3.34E-05	33.36	1.1956	48.98	1.3860	56.78	1.7504	71.71
		Total Length (u)	443.11		509.83		540.32		599.96

Fig. 2.8 Excel spreadsheet used to design filters. User inputs microstrip widths (in accordance with fabrication tolerances), substrate relative permittivity and thickness and the cut off frequency. Spreadsheet gave the length of each section for various G-values.

2.3.3 Filter Simulation

Several viable commercial packages exist for simulating the filter design namely Aplac, Serenade and HFSS. Aplac and Serenade are circuit simulators that will determine the S-parameters, e.g. S_{21}, of a two port network containing several microstrip elements that can be assigned values of width, length, substrate thickness and cavity height. These simulators can be sweep in frequency to determine the filter's response. Fig. 2.9 shows a screen shot from Aplac displaying a 10 element microstrip filter and the frequency response.

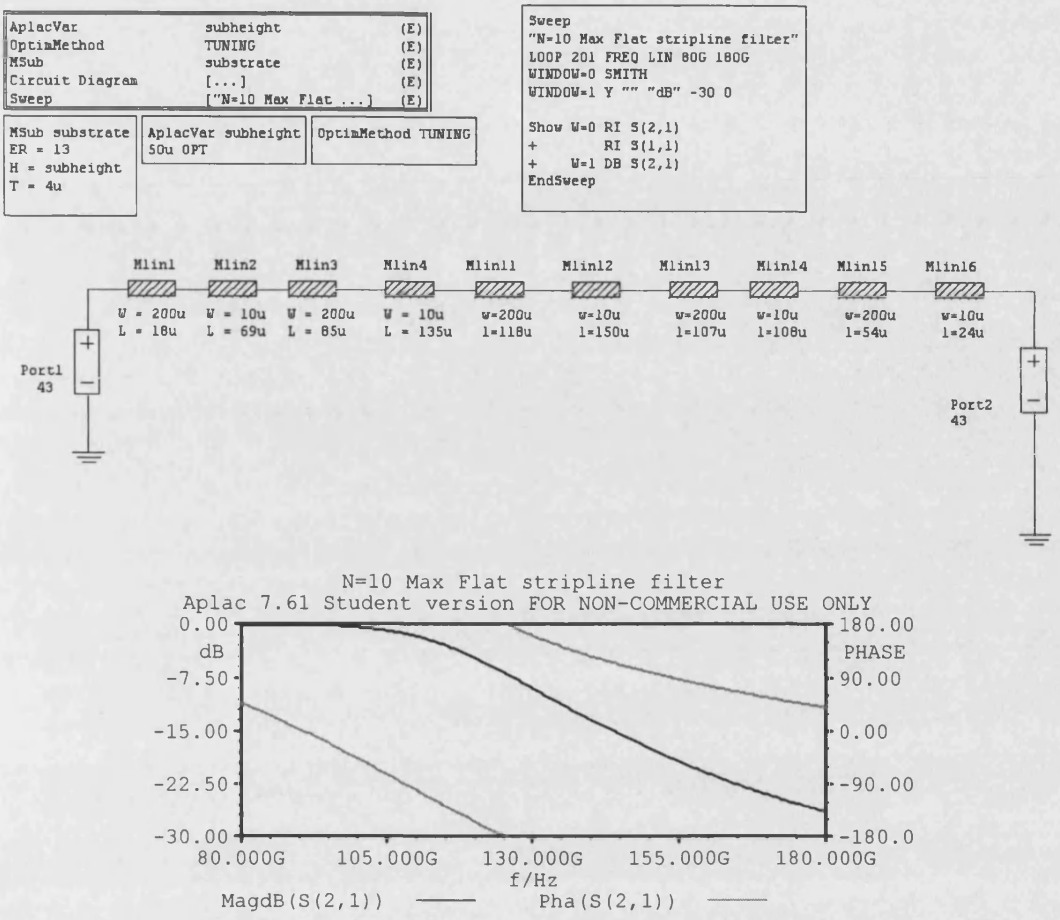


Fig. 2.9 Screenshot from Aplac's circuit simulator showing a 10 element filter and the corresponding S_{21} response through a frequency band 80 – 180 GHz.

However, these circuit simulators cannot simulate the suspended microstrip cavity that needed to be implemented in this design. The suspended cavity was needed because the GaAs substrate was thinned down to a membrane. If used in a normal cavity designing the filter would be very difficult due to the small distance between the microstrip and the ground plane. The suspended cavity modifies the effective permittivity between the conductor and the ground plate. Ansoft's HFSS was used to determine the response characteristics of the filter within the suspended cavity. A parametric analysis was then implemented to fine tune the filter.

2.3.4 Scale Model Filter

As part of the scale modelling done (see Chapter 5) a filter was needed with a cut off frequency of 3.1 GHz and an insertion loss greater than 15 dB between 4 and 7 GHz. The spreadsheet in Fig. 2.8 was used to design a 9 element low-pass filter with

minimal ripple in the pass band. Fig. 2.10 shows the Aplac response for the filter designed in the spreadsheet. Fig. 2.11 shows a picture of the fabricated filter and the filters measured response is shown in Fig. 2.12. The difference between the measured and simulated results can be explained by the lack of controllable variables in the model and the tolerances in the fabrication of the filter not matching those of the design.

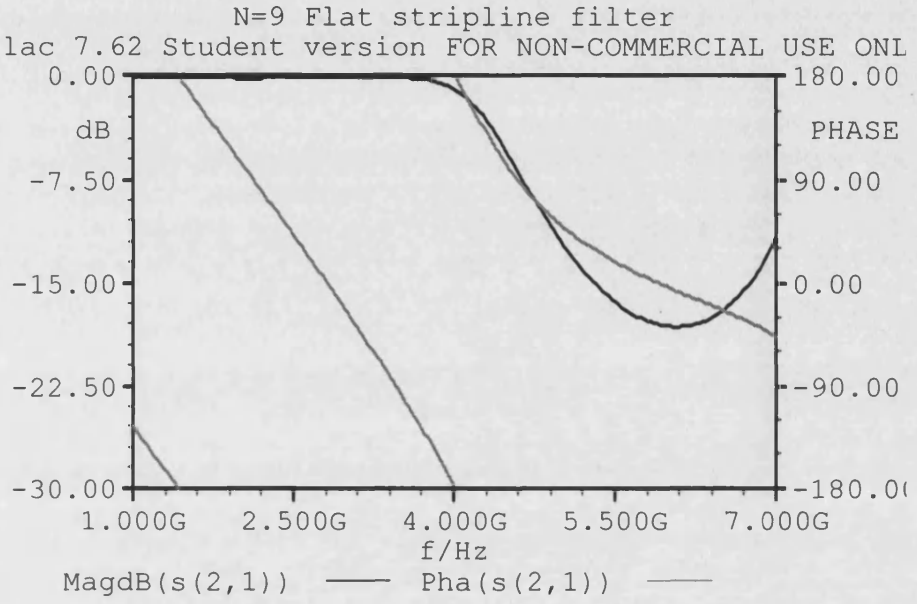


Fig. 2.10 Frequency response of the 9 element low-pass filter in Aplac.

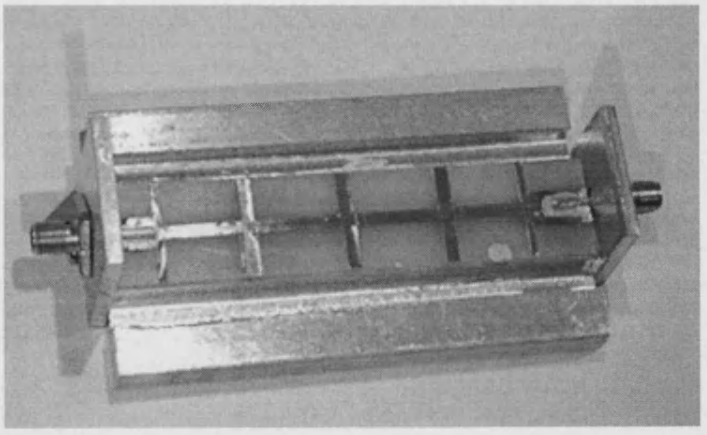


Fig. 2.11 A 9 element filter fabricated with copper conductor on a plastic substrate in an aluminium cavity and connected using standard 50 Ω SMA connectors.

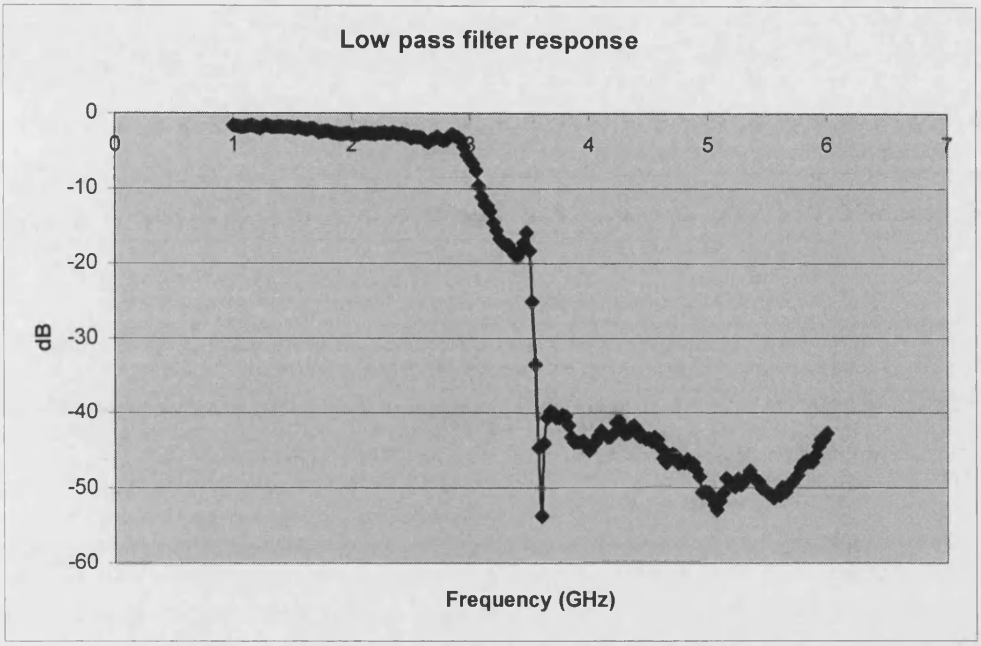


Fig. 2.12 Response of the fabricated filter clearly showing minimal loss in the pass-band and good insertion loss above 3.1 GHz.

2.4 High Frequency Backshorts

Backshorts fall into two main categories: fixed and tuneable. A fixed backshort usually means that the circuit cannot be tuned and will therefore be less broadband. However, tuneable backshorts are difficult to make and increasingly so with higher frequencies. A fixed backshort was chosen to operate at optimum output frequency of 200 GHz. Steps were taken in the design to ensure the multiplier could be as broadband as possible without using movable backshorts.

Viewed electrically the backshort is simply a terminated transmission line. Fig. 2.13 shows a lossless transmission line of characteristic impedance Z_0, terminated in a load impedance Z_l at position z = 0. From [2.10] it can be shown that

$$Z_{in} = Z_0 \frac{(Z_l + Z_0)e^{j\beta l} + (Z_l - Z_0)e^{-j\beta l}}{(Z_l + Z_0)e^{j\beta l} - (Z_l - Z_0)e^{-j\beta l}} \tag{2.17a}$$

$$= \frac{Z_l \cos \beta l + jZ_0 \sin \beta l}{Z_0 \cos \beta l + jZ_l \sin \beta l} \tag{2.17b}$$

$$= \frac{Z_l + jZ_0 \tan \beta l}{Z_0 + jZ_l \tan \beta l}. \tag{2.17c}$$

As previously mentioned the backshort is a terminated transmission line and for the purpose of this proof it is assumed that a backshort can be made with zero impedance, i.e. $Z_l = 0$.

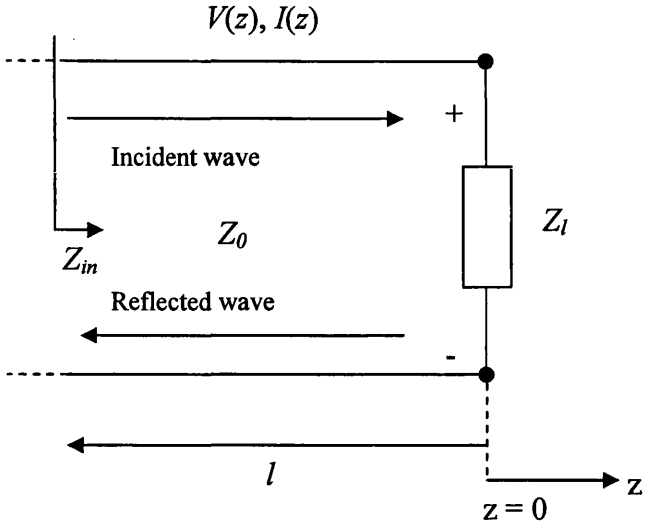


Fig. 2.13 A terminated transmission line with characteristic impedance Z_0. A load impedance Z_l terminates a lossless transmission line of length l.

This implies the terminated line is a short circuit and (2.17) can be reduced to

$$\frac{Z_{in}}{Z_0} = jZ_0 \tan \beta l \qquad (2.18)$$

which is purely reactive for any length of transmission line. The impedance is zero at $l = 0$ and open circuit at for $l = \lambda/4$, this is repeated every $\lambda/2$. Fig. 2.14 shows the voltage, current and input impedance for the short circuited line.

Equation (2.18) can be used at a distinct advantage when designing a multiplier. The largest contributor to conversion loss in a multiplier is the large parasitic capacitance of the varactor diodes which is covered in section 4.3.3. Due to the tan function of (2.18) the reactance on the transmission line can be tuned to be positive and hence inductive at periodic locations. It follows then that a multiplier may be designed so that the backshort resonates out the parasitic capacitance of the diode. Practically, backshorts are impossible to fabricate with absolutely zero impedance and therefore

have a parallel resistive component to either a capacitive or inductive element determined by *l*. Fig. 2.15 shows a simplified schematic of a backshort tuning circuit.

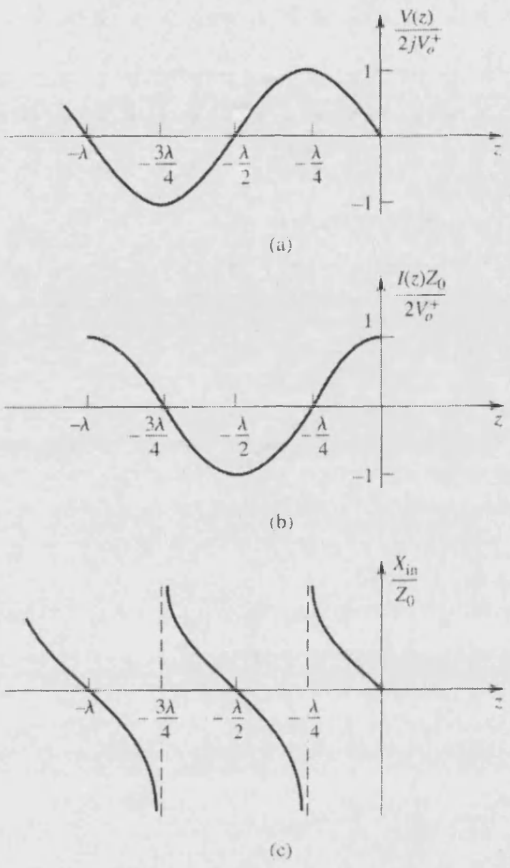


Fig. 2.14 Graphs showing the (a) voltage, (b) current and (c) impedance as a function of short circuited transmission line length, [2.10].

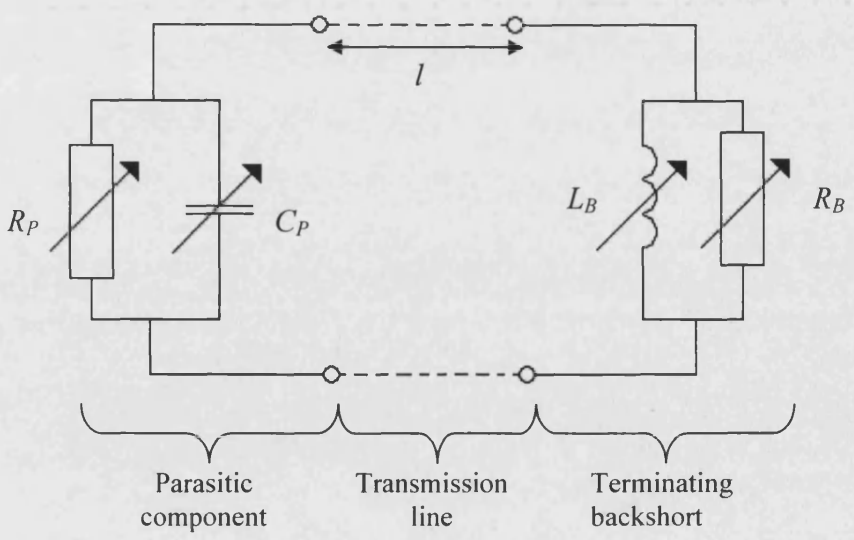


Fig. 2.15 Simple circuit diagram to show the principle behind backshort tuning. The correct distance, *l*, needs to be found between the terminating short circuit and the parasitic component C_P so that the backshort impedance appears inductive, L_B, and resonates out the reactance in the circuit.

For the backshort in Fig. 2.15 to completely resonate out the parasitic capacitance the backshort should be the correct distance, l, from the parasitic component. This will happen when, for example, the parasitic component is a distance $\lambda/4$ from the terminating short and the backshort will appear inductive. For the effect of the parasitic components to be removed completely then the backshort reactance must be equal and opposite to the parasitic reactance, i.e.

$$j\omega L_B = -\frac{j}{\omega C_P}. \tag{2.19}$$

This is a highly simplified example to demonstrate how the backshort is used for tuning and the theoretical underpinning.

Fig. 2.16 shows an E field plot for a WR10 waveguide in the first TE mode which terminates (at z = 0) in a short circuit. This graphically shows what was calculated in Fig. 2.14a.

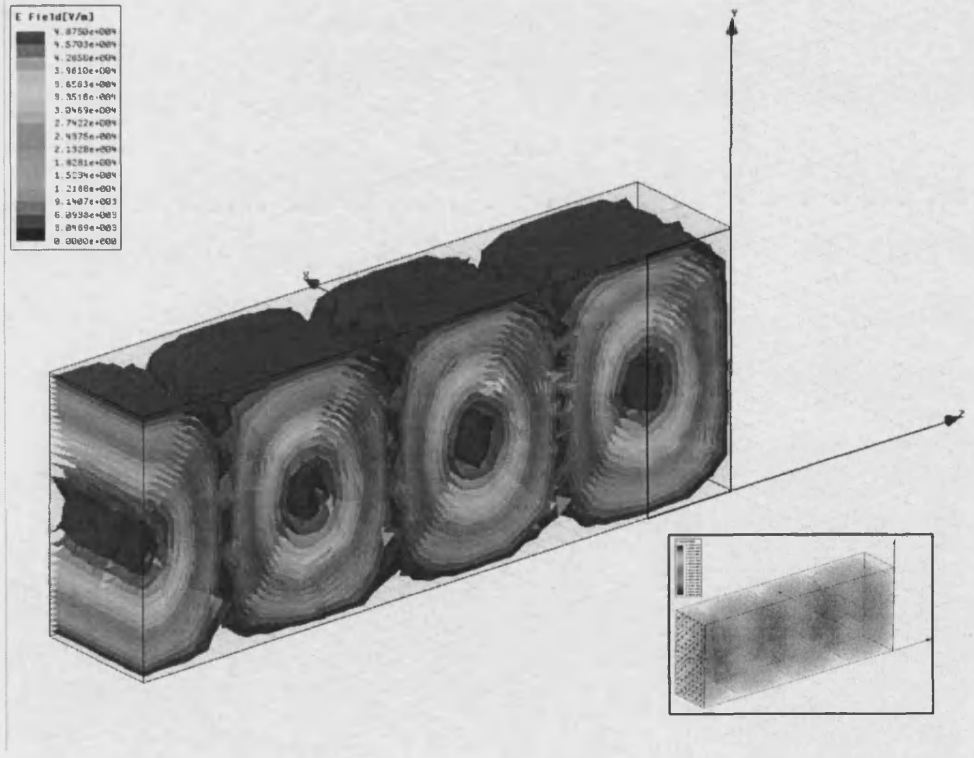


Fig. 2.16 Graphical representation of electric field strength of a standing wave formed from a waveguide transmission line being terminated in a short circuit. Inset indicates position of wave port.

The waveguide in Fig 2.16 (has dimensions 2.54 x 1.27 x 6.5 mm) supports single mode frequencies in the band 75 – 110 GHz and the plot simulates a 100 GHz signal. In order to determine the true λ/4 distance in a waveguide at 100 GHz the guided wavelength must be calculated. From [2.10] it follows that the guided wavelength is given by

$$\lambda_g = \frac{2\pi}{\sqrt{\left(\omega\sqrt{\mu\varepsilon}\right)^2 - (m\pi/a)^2 - (n\pi/b)^2}} \tag{2.20}$$

for a TE_{mn} mode wave in a waveguide of dimensions a x b where b ($a > b$) is the waveguide height, μ is the permeability and ε is the permittivity of the waveguide dielectric (in this case a vacuum).

For a 100 GHz signal in a WR10 waveguide the guided wavelength is $\lambda_g = 3.71$ mm and the distance from the terminating wall (or backshort) to the first area of high density electric field is therefore at z = 0.92 mm (this is indicated with black line across the broad wall of the waveguide in Fig. 2.16).

2.5 Bandwidth and Loss

Diodes and other passive circuit components in multipliers are essentially lossy components. As a result a multiplier will always have a conversion loss which is a logarithmic ratio of input and output power given by [2.2],

$$L = 10\log_{10}\left(\frac{P_{in}}{P_{out}}\right) \text{ dB} \tag{2.21}$$

where L is the loss in dB (decibels), P_{in} is the power at the source, P_{out} is the output power. A common goal when designing a multiplier is to maximize the efficiency, or minimise the conversion loss, which was one of the goals of this project. The backshort, usually a metal sliding plug in a waveguide cavity, maybe tuned by moving its position in and out of the waveguide which also contributes to minimising conversion loss (as described above). Tuning the backshort of a non-optimized

multiplier will increase the efficiency at a single frequency and therefore the bandwidth around that frequency. Bandwidth is defined as the output frequency range over which a suitable degree of efficiency is attained usually 3 dB. Fig. 2.17 shows a hypothetical response of a high frequency system where insertion loss, L_n, is plotted as a function of frequency. In this example the frequency bandwidth, B, is set between the limits of insertion loss, L_{nmax} and L_{nmin}.

As with most other systems that involve signal processing there is an obligatory amount of noise. Noise can enter the system at all stages, from modulation of the output of the signal generator to components of the multiplier circuit and devices. This noise along with undesired sideband components from nonlinear element mixing will be present in the output noise spectrum.

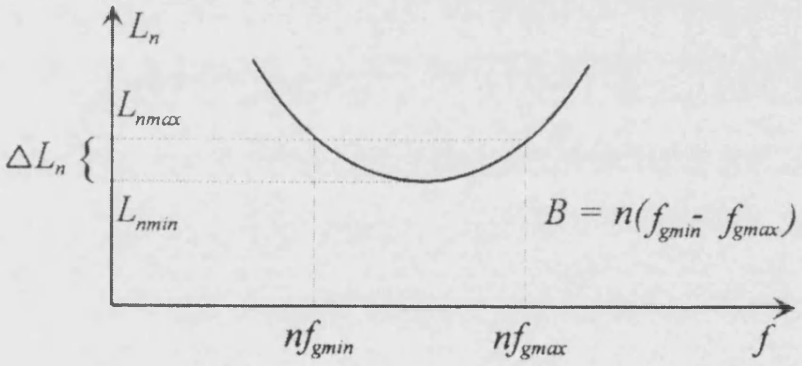


Fig. 2.17 Example of frequency multiplier bandwidth, L_n is loss at n[th] harmonic, nf_{gmin} is lower bandwidth limit, nf_{gmax} is the upper bandwidth limit, L_{nmax} and L_{nmin} are the maximum and minimum losses at the n[th] harmonic and B is the bandwidth of n[th] harmonic [2.2].

2.6 Limits of Varactor and Varistor Multipliers

An ideal varistor, being a purely nonlinear resistive device, has virtually no reactance and cannot store reactive energy. As a result, a multiplier with a varistor nonlinear element would need no input or output tuning and would yield large bandwidths. However, due to varistor multipliers being resistive they dissipate a lot of energy and are extremely inefficient. Page [2.11] originally stipulated the following relationship for varistor multipliers with no sidebands and input power equal to signal generator power,

$$L \geq n^2 \tag{2.22}$$

where n is the order of the multiplication. This evidently shows the huge conversion losses through varistor multiplying increases as the square of the order regardless of other loss factors such as waveguides, internal generator loss etc.

Varactors are, ideally, purely reactive elements, (part of the design optimisation of this project was to minimise the real component of the devices impedance), and do not dissipate energy. However, to exploit this very desirable property it was necessary to ensure adequate impedance matching. This included the tuning out of unwanted circuit reactances such as the inherent parasitic capacitance of the varactor diode. As a consequence of this fixed-tuned circuit there are severe limitations on the bandwidth of the multiplier. It is desirable to maximise the bandwidth of a multiplier and this was also in the design criteria of this project.

2.7 Burckhardt Approach

Theoretical frequency multiplier design was spearheaded in 1965 in a paper by Burckhardt, [2.12]. The model used in the theory assumes the varactor to be a variable capacitance in series with a constant resistance, R_s. Further modelling is done with a variable resistance but all results are the same as in the case with R_s constant, with the exception of some modifications to the efficiency. The model restricts the range of voltage across the junction between the barrier potential, Φ_b, and the reverse breakdown voltage, V_b. If the applied voltage is at these limits then the diode is fully driven and beyond these limits the diode is overdriven. The model also assumes that during forward conduction the voltage is fixed at Φ_b and it is the charge that continues to rise. Burckhardt acknowledges this will lead to infinite capacitance and suggests that the model is used only when the period of forward conduction is several times smaller than the time taken for an *appreciable* number of minority carriers to recombine. He assumes losses only come from the diode junction and that currents only flow at input, output and, if necessary, idler frequencies. Hence the use of filters, matching networks and harmonic suppression (through anti-series or anti-parallel diode configurations) were used to prevent currents at undesired frequencies from flowing.

The analysis starts with an expression for the voltage dependent charge across the junction given by [2.12],

$$\left(\frac{V_j - \Phi_b}{V_b - \Phi_b}\right) = f\left(\frac{q - q_\Phi}{Q_B - q_\Phi}\right) \tag{2.23}$$

where V_j is the voltage across the junction, q is the charge on the junction, Q_B is the charge at breakdown and q_Φ is charge at contact potential. The model describes the input, S_{01}, and output, S_{0N}, elastance (the inverse of capacitance) of the multiplier. The analysis arrives at the definition of the normalized drive level defined as,

$$D = \frac{Q_{max} - Q_{min}}{Q_B - q_\Phi} \tag{2.24}$$

where Q_{max} and Q_{min} are the maximum and minimum junction charges respectively. If $Q_{max} = q_\Phi$, the drive level is as great as it can be without causing diffusion charge storage and hence $D = 1.0$. When overdriven, $D > 1.0$, a degree of diffusion storage charge is eminent. Results of the analysis are given in table form, an example for a frequency doubler is given in Table 2.1.

$\gamma =$	*0.0*		*0.333*			*0.4*			*0.5*	
D =	1.5	2.0	1.0	1.3	1.6	1.0	1.3	1.6	1.3	1.6
α	6.7	4.7	12.6	8.0	6.9	11.1	8.0	7.2	8.3	8.3
β_1	0.022	0.062	0.011	0.032	0.058	0.016	0.040	0.067	0.055	0.083
S_{01}/S_{max}	0.73	0.50	0.68	0.52	0.40	0.61	0.45	0.35	0.37	0.28
S_{02}/S_{max}	0.60	0.50	0.66	0.48	0.41	0.59	0.44	0.38	0.40	0.34
V_{0norm}	0.35	0.25	0.41	0.33	0.27	0.39	0.31	0.26	0.28	0.24

Table 2.1 Design parameters for a frequency doubler, [2.12]

Table 2.1 shows design parameters for abrupt, $\gamma = 0.5$, and graded, $\gamma = 0.333$, diode junctions. The parameters α and β_1 are used to determine efficiency and output

power. S_{max} is the maximum elastance, or 1 / C_{min} where C_{min} is the capacitance at V_b. V_{0norm} is the normalized bias voltage. The efficiency is given by [2.12],

$$G = \exp(-\alpha / Q_\delta) \tag{2.25}$$

where,

$$Q_\delta = S_{\max} / \omega_1 R_s \tag{2.26}$$

and R_s is the diode series resistance, ω_1 is the input radial frequency. Output power is given by,

$$P_L = \beta\omega_1 \left(\frac{\Phi_b - V_b}{S_{\max}} \right). \tag{2.27}$$

The normalized bias voltage is given as,

$$V_{0norm} = \left(\frac{\Phi_b - V_{dc}}{\Phi_b - V_b} \right) \tag{2.28}$$

where V_{dc} is the DC bias voltage. Looking at Table.1, one might assume that the highest efficiency would come from a junction with $\gamma = 0$ which corresponds to a step in elastance from S = 0 (C = ∞) to some constant at the junction boundary. This arises from the assumption made earlier that the voltage in forward conduction increases to and holds at Φ_b, at which point the capacitance becomes infinite. This is obviously not what happens in reality and a correction for the rectified forward current needs to be made. Current travelling forwards across the junction will behave as current through a varistor, i.e. the device now becomes a nonlinear resistor and consequently any voltage drop across it will dramatically add to the conversion loss.

References – Chapter 2

[2.1] M. E. Hines, "The virtues of nonlinearity – detection, frequency conversion, parametric amplification and harmonic generation," *IEEE Trans. on Microwave Theory and Techniques*, vol. MTT-32, no.9, September 1984, pp. 1097-1104.

[2.2] M. T. Faber, J. Chramiec, M. E. Adamski, "Microwave and millimeter diode frequency multipliers," *Artech House, Inc, MA*, 1995.

[2.3] X. Shiwei, "A design of a millimeter doubler," *3rd Int. Conf. on Microwave and Millimeter Wave Technology Proceedings*, 2002, pp. 959-961.

[2.4] N. R. Erickson, *et al.*, "High efficiency MMIC frequency triplers for millimeter and submillimeter wavelengths," *IEEE MTT-S WE4C-5 Digest*, 2000, pp. 1003-1006.

[2.5] N. Erickson, "High efficiency submillimeter frequency multipliers," *IEEE MTT-S Digest PP-1*, 1990, pp. 1301-1304.

[2.6] J. Archer, *et al.*, "High-output, single- and dual-diode, millimeter-wave frequency doublers," *IEEE Trans. on Microwave Theory an Techniques*, vol. MTT-33, no. 6, June 1985, pp. 533-538.

[2.7] C. Tripon-Canseliet, A. Maestrini, I. Mehdi, "Design of a wideband 900 GHz balanced frequency tripler for radioastronomy," *Joint 29th International Conference on Infrared and Millimeter Waves and 12th International Conference on Terahertz Electronics*, September 2004, pp. 583-584.

[2.8] G. L. Matthaei, L. Young, E. M. T. Jones, "Microwave filters, impedance matching networks and coupling structures," McGraw-Hill, New York, 1964.

[2.9] D. W. Porterfield, *et al.*, " A high-power fixed-tuned- millimeter-wave balanced frequency doubler," *IEEE Trans. on Microwave Theory and Techniques*, vol. 47, no. 4, April 1999, pp. 419-425.

[2.10] D. M. Pozar, "Microwave engineering," John Wiley and Sons Inc., New York, 1998.

[2.11] C. Page, "Frequency conversion with positive nonlinear resistors," *J. Res. Nat. Bur. Stand.*, vol. 56, April 1956, pp. 179-182.

[2.12] C. B. Burckhardt, "Analysis of varactor frequency multipliers for arbitrary capacitance variation and drive level," *Bell Systems Technical Journal*, vol. 44, April 1965, pp. 675-692.

Chapter 3

Literature Review

This review describes the development of frequency multipliers, the evolution of the nonlinear devices used in the circuitry and how other improvements such as low-loss circuit mounts have increased output power and efficiency over the last 30 years. Frequency multipliers in the millimetre wave region of the spectrum initially used whisker contact varactor diodes as the nonlinear element. Over the years this has developed to the planar structure commonly used today. Also discussed are other novel nonlinear elements such as the Heterostructure Barrier Varactor (HBV) and the metal/ 2-DEG (2-Dimensional Electron Gas) Schottky diode. Also discussed are diode arrays for increased power handling and integrated diodes structures with membrane substrates.

3.1 Literature Review

Although not strictly in the frequency range of interest, Rafuse and Steinbrecher [3.1] introduced the first multiplier to use a waveguide structure in 1965. The multiplier schematic is shown in Fig. 3.1 displaying a cross-section of the waveguide with bias and tuning stubs. The Authors claimed, at the time, that this multiplier was the first to use a diode pair configuration to successfully separated the even and odd harmonic power. The circuit was tuned for input, output and idler frequencies using a pair of tuning stub circuits. The quadrupler had a peak output power of 50 mW at 22 GHz and a peak efficiency of 18.5% which is shown in Fig. 3.2. The multiplier had two GaAs varactor diodes situated in the output waveguide and boasted impressive performance for such an early design.

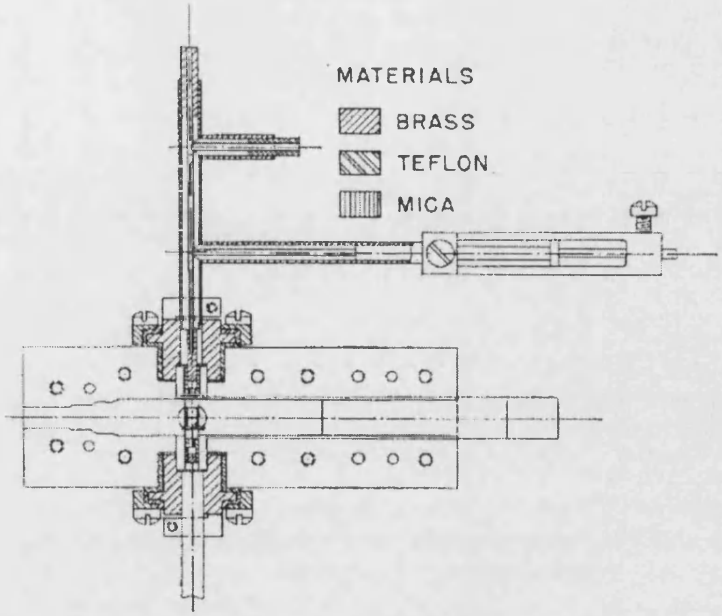


Fig. 3.1 Schematic of 22 GHz quadrupler showing detail of a single idler circuit and the open topped waveguide block. Quarter-wave tuning stubs, for idler frequencies, are shown in upper part of diagram connected to the multiplier block where the pair of GaAs varactor diodes were situated in the waveguide itself [3.1].

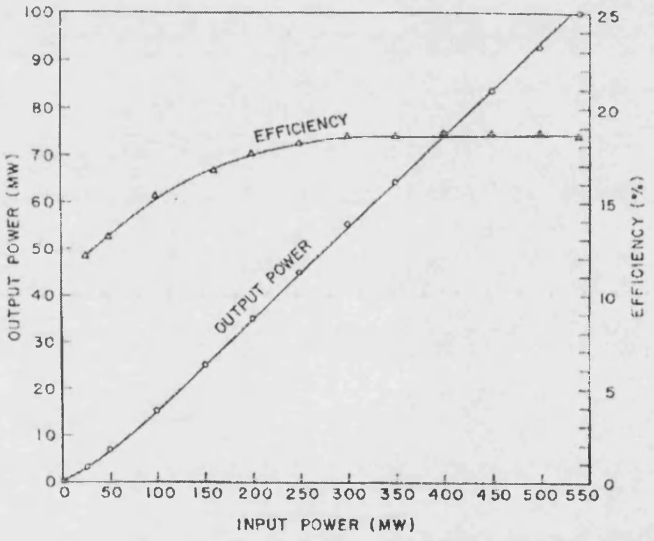


Fig. 3.2 Efficiency and power output as a function of input power for the quadrupler. Bias tuned for each measurement [3.1].

Cohen *et al* [3.2] introduced one of the first multipliers that operated above 100 GHz. The first of two multipliers described as a *dominant mode double ridge type structure* successfully doubled a 100 GHz signal to an impressive 10.2 mW with a peak efficiency of 12.3%. Using this same style multiplier mount, a tripler to 300 GHz delivered 1.2 mW and 1.4% peak efficiency. Cohen also introduced a novel quasi-optical monopole double mesa. This is essentially a rectangular platform in a

waveguide where two diode chips are situated. It appears that the devices and the dipole elements act as an antenna coupling power in from one direction of the waveguide at the fundamental and transmitting it at the second harmonic through a 200 GHz resonant iris. The monopole quasi-optical doubler can be see in Fig. 3.3 showing the resonant irises and the dipole elements. Cohen claimed 10.1 mW of output power and 8.6% peak efficiency at 200 GHz for the quasi-optical monopole doubler. Doubler output power and efficiency results for this multiplier are shown in Fig. 3.4.

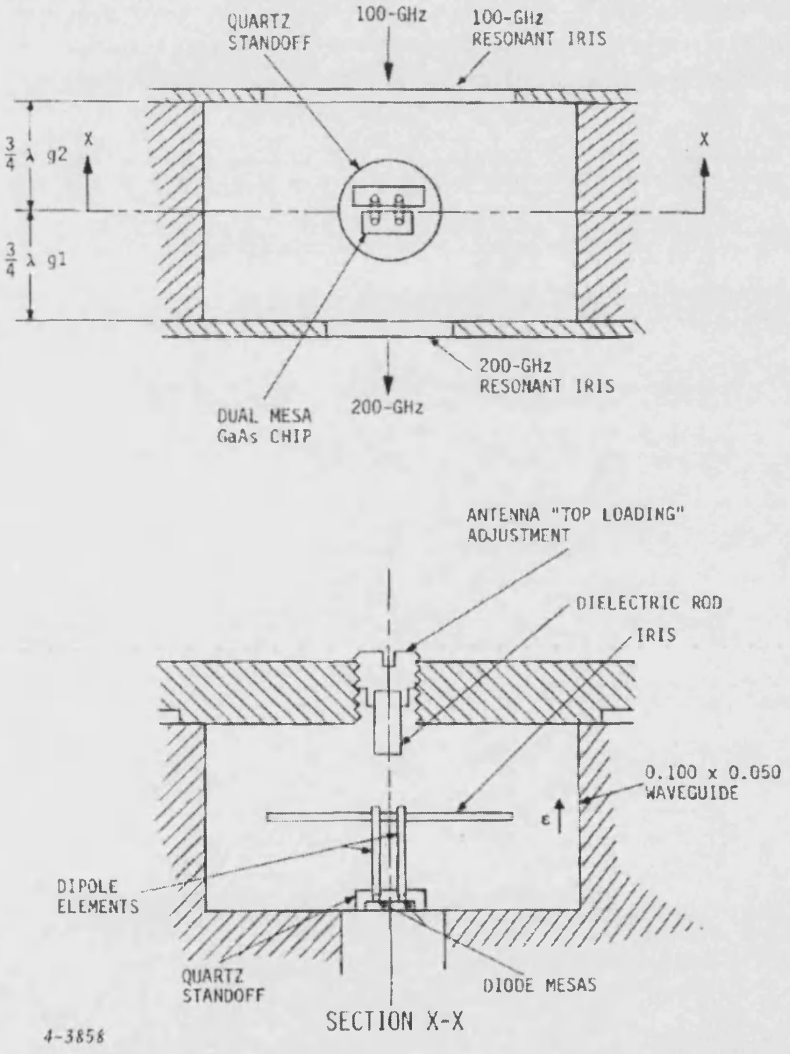


Fig. 3.3 Monopole quasi-optical doubler showing dual mesa chip and resonant iris acting as fundamental filter [3.2].

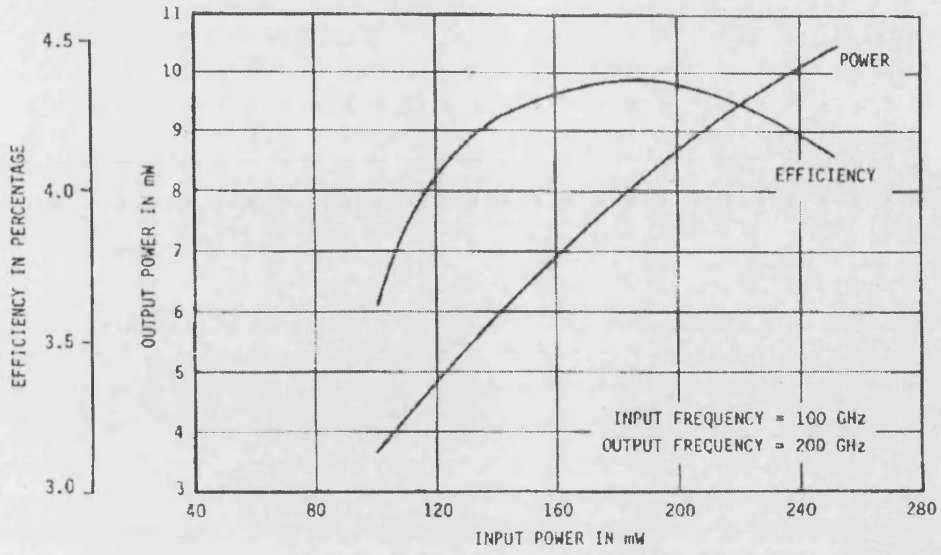
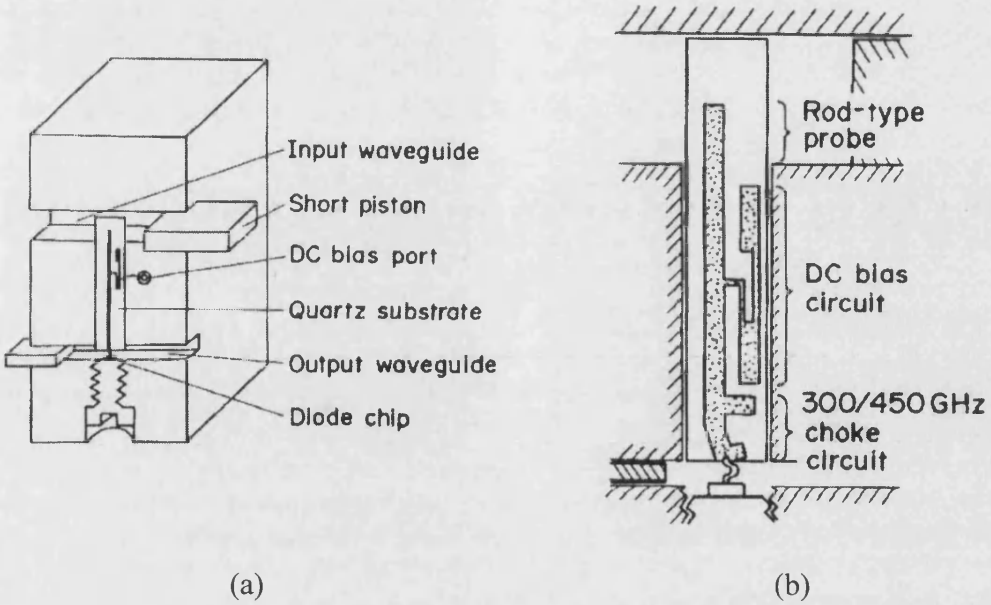


Fig. 3.4 Efficiency and output power as a function of input power for the quasi-optical monopole doubler utilizing two varactors [3.2].

In 1978 Hirayama *et* al [3.3] introduced the first whisker contacted crossed waveguide multiplier which was the design to be followed for the next 9 years until the introduction of the planar diode. Fig. 3.5 gives a cross-sectional and close up view of the frequency multiplier designed by Hirayama. A substrate with microstrip transmission line coupled power from an input waveguide through a cavity to a whisker where it contacted a diode chip situated in the output waveguide. Filter stubs inside the cavity provided RF isolation of the DC connection. Two subsequent papers [3.4] and [3.5] showed developments in diode modelling and improved circuit matching of this design which can be seen in Fig. 3.6. Modelling of the RF power and embedding impedance were also used to improve the multiplier performance. The groups original doubler to 300 GHz attained a peak output power of 0.6 mW and 5.2% peak efficiency escalated to 5.0 mW output power and 9.3% efficiency through implementation of the optimising methods. The tripler to 450 GHz [3.3] saw a 0.35 mW increase in power output (0.1 mW to 0.45 mW) and a 7% (1.1% to 8.1%) increase in efficiency as a result of the same modifications.



(a) (b)

Fig. 3.5 (a) Inner view of multiplier structure and (b) top view of substrate showing tuning stubs and whisker contact to diode chip [3.3].

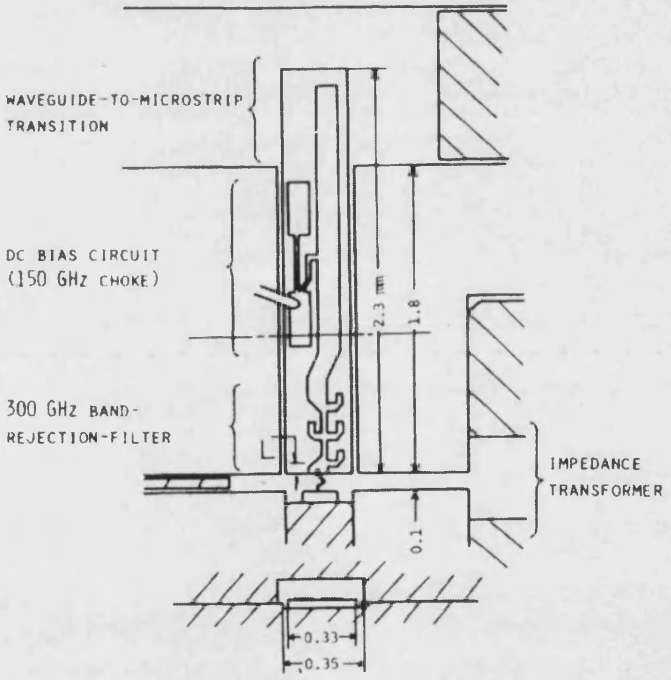


Fig. 3.6 Top view of modified substrate with refinements to tuning stubs and DC isolation [3.5].

Archer [3.6], following Takada's crossed waveguide design, introduced a mechanically tuneable broadband doubler with an output range 110 -170 GHz. The crossed waveguide design is shown in Fig. 3.7. Fig. 3.7 shows the split block, input waveguide with backshort, the coaxial bias connector, output waveguide and location

of the whisker contacted diode. The upper inset of Fig. 3.7 shows the detail of the quartz substrate which has the low pass filter and the input waveguide probe. The inset shows a bypass capacitor which is situated a quarter wavelength, at the input frequency, from the main transmission line and prevents RF power at the input frequency from passing down the bias line. It is also clear that the diode is situated in the output waveguide and connected by a whisker pin which is spanning it. The multiplier produced 8 mW of output power and 10 % efficiency over the entire range indicated. The results of the frequency dependent output power of the multiplier are shown Fig. 3.8. This was the first demonstration of a single whisker contacted diode with such broadband output and as a result the crossed waveguide design became very popular. In the same paper Archer also reported a tripler to 215 GHz with 4.8 mW output power and 6 % efficiency.

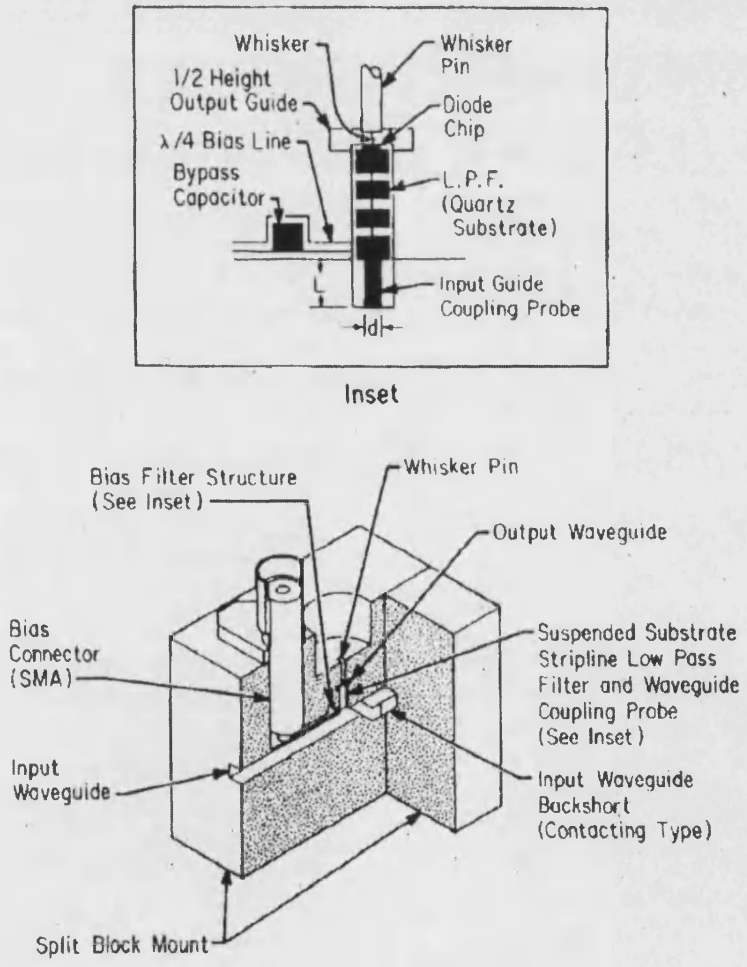


Fig. 3.7 Crossed waveguide structure with inset showing detail of filter and whisker pin [3.6].

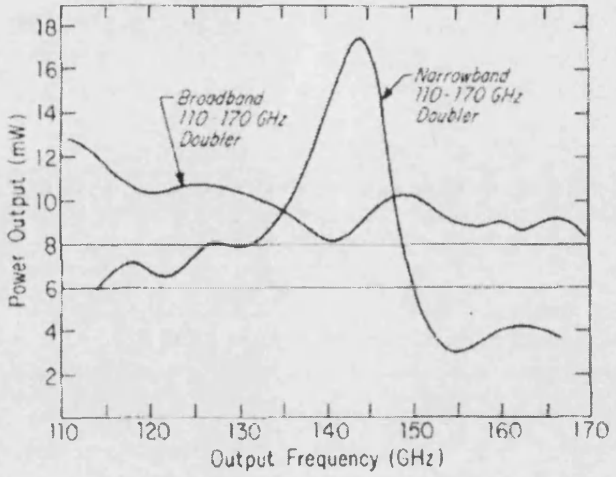


Fig. 3.8 Performance of the 100 – 170 GHz output frequency multipliers [3.6].

Archer improved the cross-waveguide mount, matching circuit and waveguide to stripline coupling in a doubler to the 80 – 120 GHz band, [3.7]. This multiplier produced a peak output power of 12 mW and an efficiency ≥ 5.6 % between 90 – 124 GHz (6 % peak) when properly tuned at discrete frequencies. Results of the output power as a function of frequency are shown in Fig. 3.9.

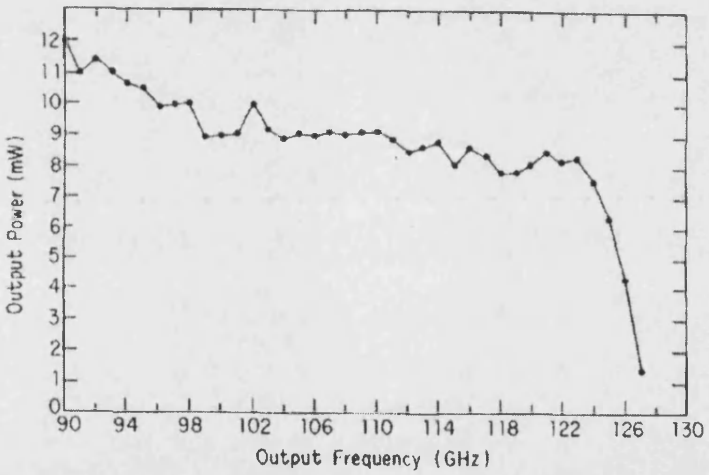


Fig. 3.9 Doubler performance between 90 and 130 GHz with optimised backshort and bias for each measurement [3.7].

Erickson, soon to lead the field alongside Archer and others, introduced a tripler to the 195 – 235 GHz band, [3.8], again using the cross-waveguide mount, whisker contacted diode and coaxial resonator acting as a low-pass filter claiming easier construction and implementation over microstrip on quartz filters. A cross-section

schematic of Erickson's frequency multiplier is shown in Fig. 3.10. The peak power output was 4 mW and had a peak efficiency of 10.5 %, results shown in Fig. 3.11.

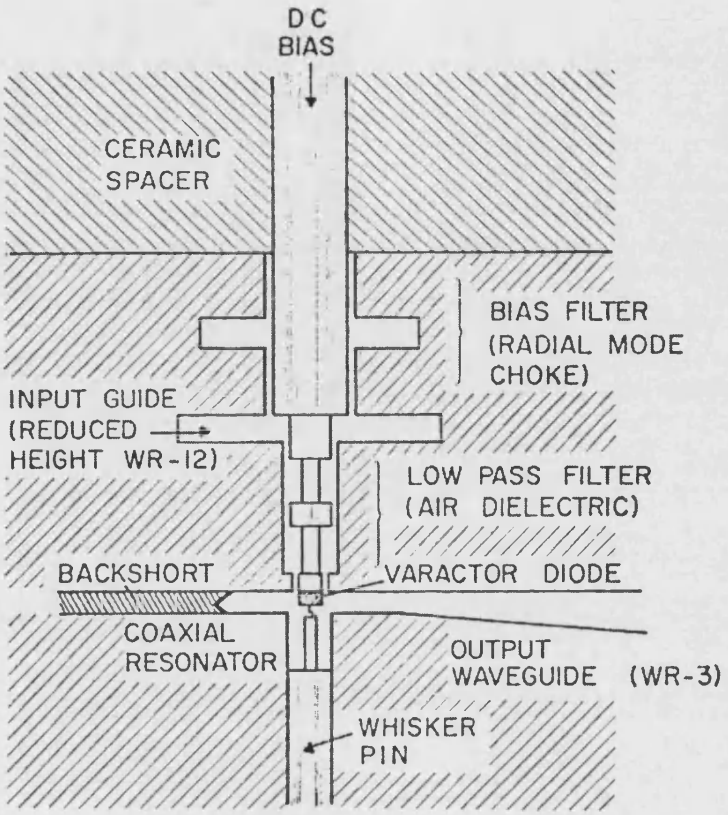


Fig. 3.10 Cross-section through the 230 GHz tripler showing coaxial low pass filter and varactor diode chip situated in reduce height WR-3 output waveguide [3.8].

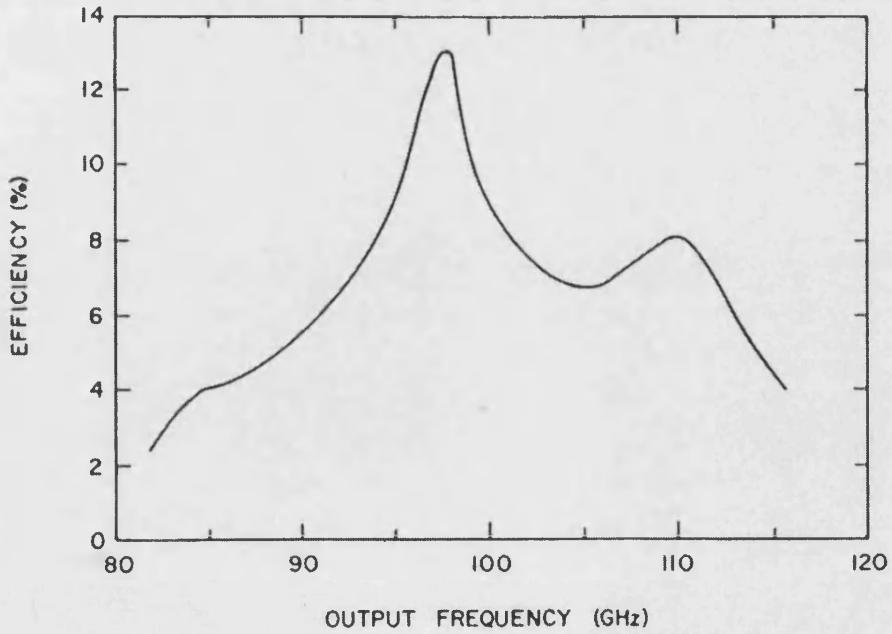


Fig. 3.11 Efficiency as a function of output frequency for the 230 GHz tripler [3.8].

Archer then introduced a tripler to the 200 – 290 GHz band [3.9] which incorporated a novel suspended microstrip, new low-pass filter and optimised waveguide transformer. Peak output power was ≥ 2 mW over the entire band and peaks at 4.8 mW and 8 % efficiency, surpassing all previous results. In another paper from Archer at around the same time [3.10], a tripler to the frequency band 260 – 350 GHz is also reported with peak output power 3 mW and peak efficiency 3.7 % with improved filters and matching circuit. Results of this tripler are shown in Fig. 3.12.

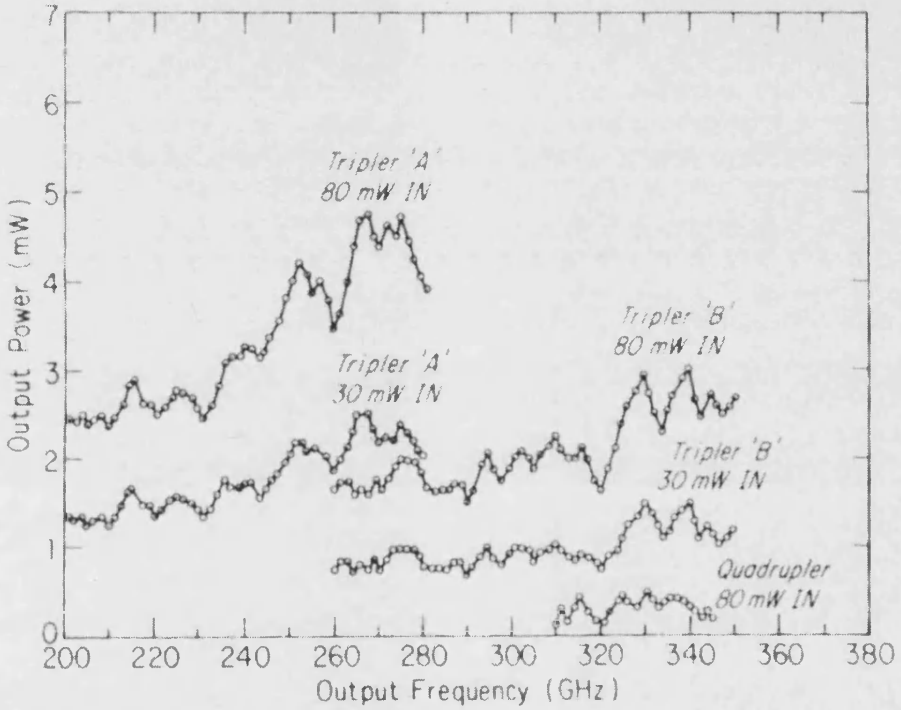


Fig. 3.12 Measured performance of several multipliers, triplers and quadruplers with different constant input powers. Tuning and bias were optimized for each reading [3.10].

In 1985 Archer and Faber [3.11] were among the first to introduce a balanced multiplier. Using a special 4-port junction, (a special low loss junction that connected four waveguides together with integrated impedance transformers) two diodes could be pumped in separate waveguides with the same input signal and the outputs of both combined and put into phase. Fig. 3.13 shows the position of the 4-port junction and the two input waveguides where two separate varactor chips on separate substrates are situated with separate bias connectors. The two diode balanced design gave > 18 mW output power across the range 85 – 116 GHz (peak 26.5 mW) and a peak efficiency of 13.9 %. This showed a marked improvement on the single diode multiplier (tested alongside the double diode) which gave > 10 mW output power over the range 85 – 116 GHz (peak 15 mW) and 16.6 % peak

efficiency. However the group reported improvements in the single diode multiplier when the varactor was replaced for another with a much higher breakdown voltage giving no less than 18 mW over 97 – 116 GHz range (peak 23 mW) and peak efficiency of 15.3 %. The doubler was then cascaded with a tripler to give > 0.6 mW over the band 310 – 350 GHz (peak 0.8 mW) and a peak efficiency of 0.42 %. This is far less efficient than directly tripling to the same band such as in [3.10].

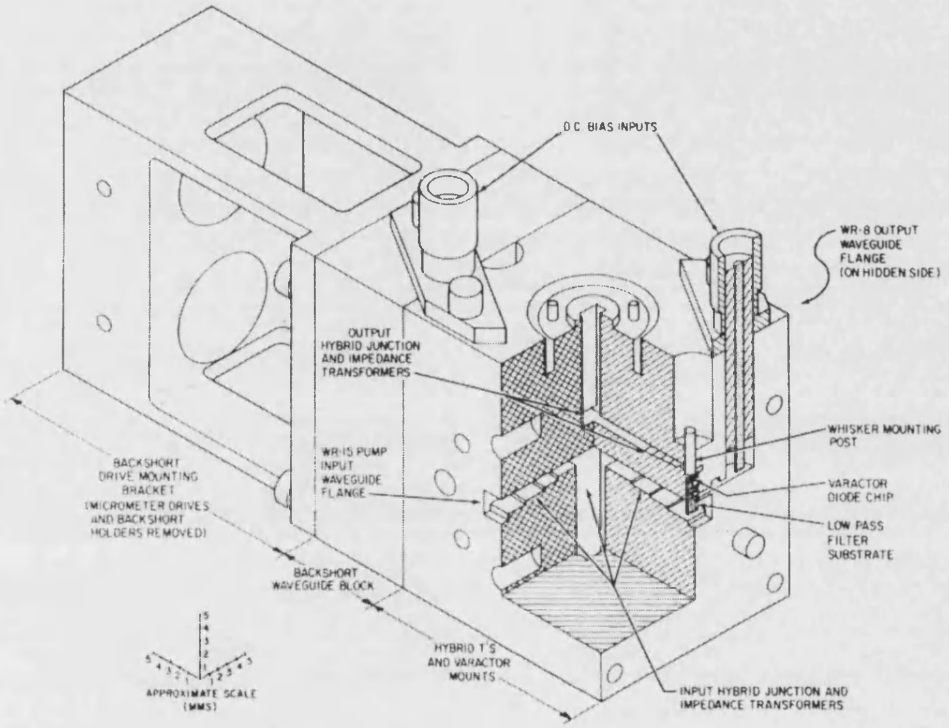


Fig. 3.13 Isometric drawing of balanced doubler design showing two input guides in 4-port configuration [3.11].

Rydberg and Gronqvist [3.12] were among the first to introduce a multiplier that utilizes the properties of the quantum well (QW) diode. The QW diode has a anti-symmetric I/V profile resulting in internal suppression of even harmonics and furthermore there is no need to bias a QW diode making them an attractive choice for multipliers. However, QW diodes are more difficult to fabricate than conventional GaAs Schottky diodes and due to the negative differential resistance (NDR) in the I/V characteristics they can be difficult to stabilize. Rydberg and Gronqvist's tripler to 250 GHz had a peak output power of 0.8 mW with 1.2 % peak efficiency, far off that attained with varactor diodes in the same frequency range although much more development had been done with GaAs diodes at this stage.

Tolmunen, Raisanen and Sironen [3.13] describe theoretical and experimental analyses of doublers and quadruplers. Optimisation was done using extensive computer analysis alongside scale modelling. The type of multiplier analysis is not specified although there are several tables and graphs showing: diode absorbed power vs. bias voltage, input power vs. output power with the effect of multiplication order and from what fundamental frequency, best theoretical efficiency and optimum embedding impedance to achieve them. The modelling results were used to construct the multiplier mounts. Experimentally the quadrupler attains 1.13 mW peak output power at 148 GHz with 11.3 % peak efficiency. Terminating the fourth harmonic of that multiplier with high inductance, a quintupler was formed with range 165 – 170 GHz, peak output power of 1.3 mW and peak efficiency of 4.2 %.

A landmark paper by Erickson in 1990 [3.14] set the benchmark for multiplier performance and a now popular design standard. By modifying a program, originally intended for optimising mixer block performance, by Siegel and Kerr [3.15] multiplier designers could optimise the embedding circuits of their multipliers. The onset of more powerful and more readily available computers meant that these complex programs could be easily run to simulate multiplier performance and more so to optimise them. This was the first important process that Erickson utilised. Secondly, and maybe building on Archer's idea, Erickson designed his circuit so that two diodes would be in anti-series configuration. This configuration suppresses odd harmonics and fewer lossy filters are needed resulting in more power available at even harmonics and less loss overall to the system. Erickson used the conventional crossed waveguide mount but with double whisker contacted diodes in the input waveguide as shown in Fig. 3.14a. Erickson also chose to use a coaxial bias filter in the design claiming easier fabrication.

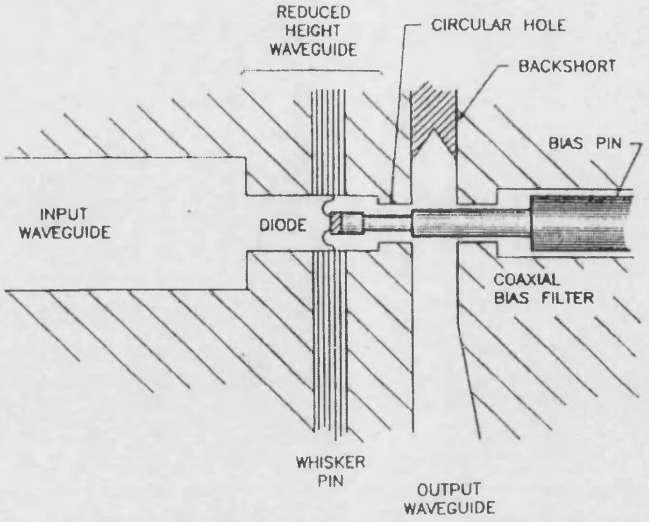


Fig. 3.14a Schematic of cross section through 160 GHz balanced doubler [3.14].

Erickson achieved an astounding peak output power of 35 mW at 188 GHz with a peak efficiency of 35%, as shown in Fig. 3.14b, much higher than Archer's dual-diode configuration at around the same frequency. On cooling to 77 K the multiplier reached an efficiency of 40%. Cascading this doubler with another similar doubler achieved a peak output power of 4 mW and peak efficiency of 3.6 % at 332 GHz, almost eight times that of Archer's design to the 300 GHz band. In the same paper Erickson reports a tripler giving 0.7 mW output power and 3 % efficiency at 474 GHz using a single diode.

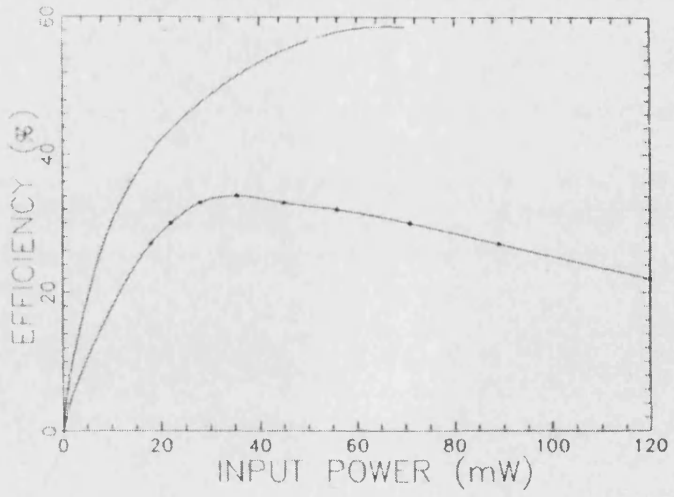


Fig. 3.14b Efficiency as a function of input power for the balanced doubler (lower curve) and theoretical (upper curve) [3.14].

Rydberg *et al.* [3.16] reported the first experimental results of frequency multiplying using a Quantum Barrier Varactor (QBV) in September 1990. The QBV, similar to the QW diode, has an anti-symmetric I/V and symmetric C/V profile. Similarly to QW diodes, even harmonics are suppressed so for designing a quintupler, as Rydberg reported here, only one idler circuit is needed at the third harmonic. They reported over 2 mW output power and 5 % efficiency across the band 210 to 280 GHz. They also compare results of a state-of-the-art Schottky diode used in the same mount, results shown in Fig. 3.15, which are comparable to that of the QBV.

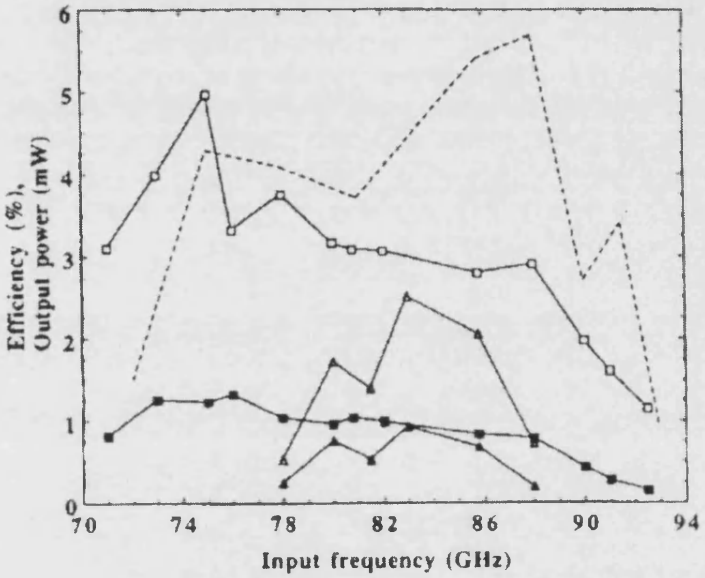


Fig. 3.15 Efficiency and output power as a function of input frequency for: upper solid line – efficiency for a 3 μm diameter QBV diode, upper broken line – efficiency for a state-of-the-art Schottky diode [3.16].

Hollung *et al* [3.17] developed a method to overcome the inherent self-heating problem associated with HBV's used in multipliers. In this novel design 15 HBV's were distributed along a finline (type of transmission line) on a quartz substrate in a WR22 waveguide as shown in Fig. 3.16. Tapered slot antennas were used to couple power in and out of the multiplier. Current density through the devices was greatly reduced due to input power being distributed between all 15 devices. This in combination with the finline structure greatly increased heat dissipation and improved efficiency. Unwanted harmonics are separated by setting the Bragg frequency of the nonlinear transmission line (NLTL). The group report a peak output power of 10 mW at 130.5 GHz with over 10 % 3 dB bandwidth and 7 % peak efficiency.

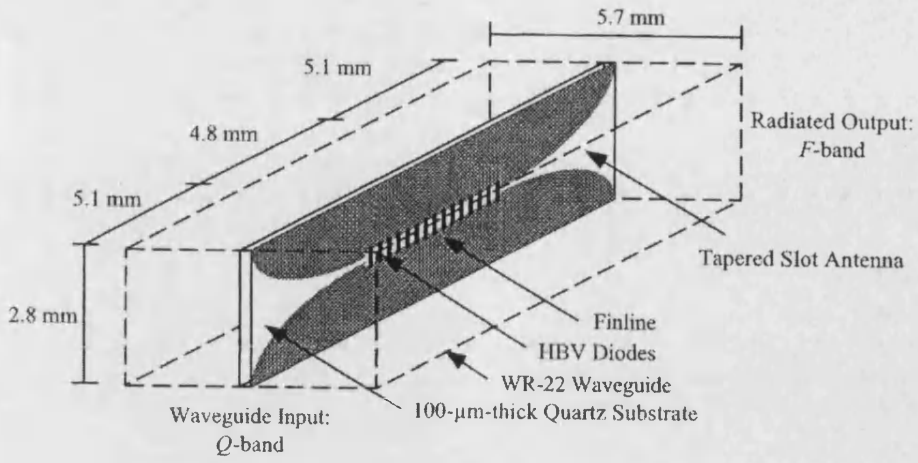


Fig. 3.16 Periodically loaded nonlinear transmission line consisting of 15 HBV diodes on a finline supported by a 100 μm thick quartz substrate with two taped slot antennas [3.17].

Around 1987 saw the introduction of the whiskerless diode, adopting the more modern planar diode structure. Planar diodes offered multiplier designers entirely new possibilities on how multipliers were constructed. The planar diode chip could be implemented more easily than the whisker diode and obviously meant that more than one diode could be used at one time without tricky construction. The planar diode also offered predictability and consistency of electrical characteristics which improved accuracy of the multiplier design. Rizzi, Crowe and Erickson were one such group to utilise these new properties, [3.18], constructing a planar chip with 4 diodes to be used in a balanced anti-series diode configuration. The extra diodes increase the power handling due to reduction in the current density through a single diode. The mount used the same crossed waveguide structure seen previously with a low pass coaxial filter and the chip mounted in the input waveguide to easily separate fundamental and harmonics. Fig. 3.17 shows the split view of the multiplier block and here the coaxial pin connects directly to the large central contact pad of the 4 planar diode array (top photo in Fig. 3.17). Apart from the planar diode much is the same as previous designs. The doubler achieved a peak output power of 55 mW and a peak efficiency of 25 % at 174 GHz.

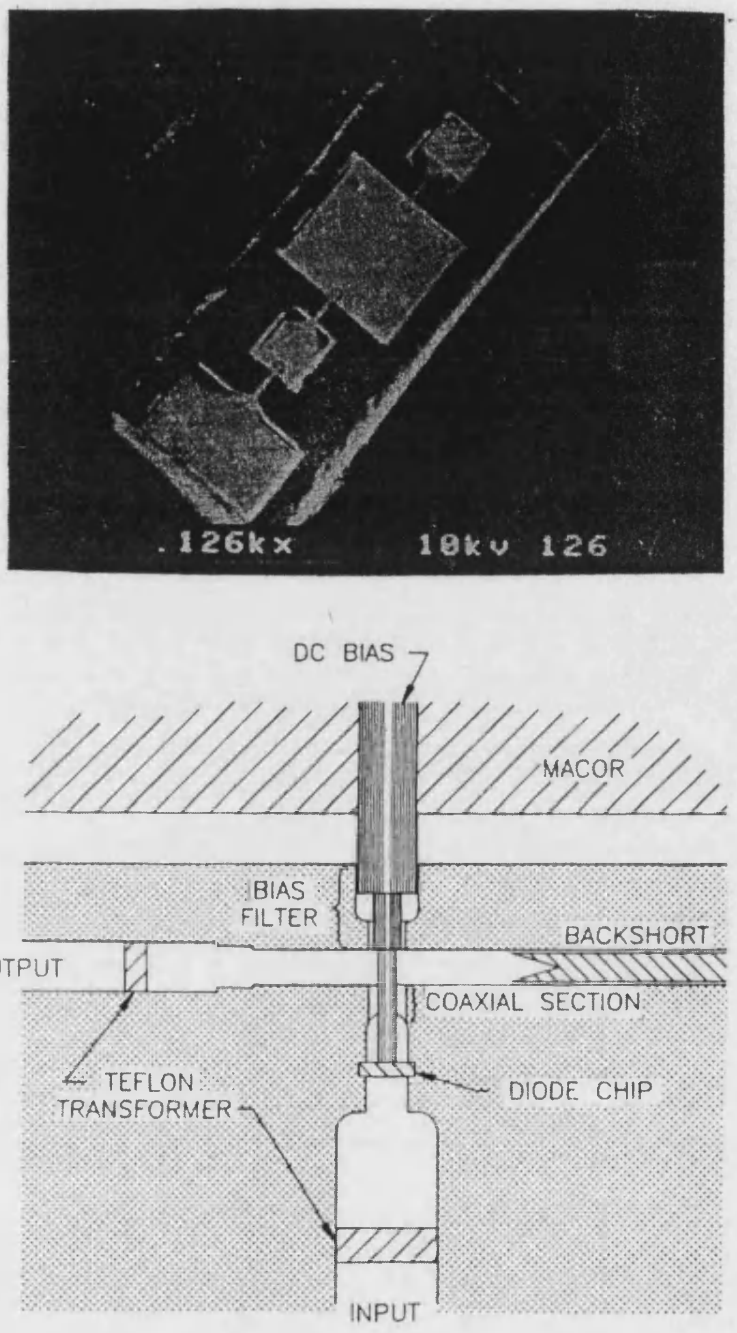


Fig. 3.17 (top) SEM photograph of balanced doubler chip with 4 anodes and large central ohmic serving as a connection pad (bottom) cross section through doubler block with diode chip in input waveguide and coaxial bias filter [3.18].

Many novel nonlinear devices have been introduced to frequency multiplier circuits as researchers looked for new ways to improve multiplier performance. Choudhury *et al.* [3.19] reported an integrated back-to-back-barrier-n-n^+ (bbBNN) varactor diode chip, shown in Fig. 3.18, for use as the nonlinear device in a frequency tripler. The idea behind this development was the reduction in chip size and integration to

microstrip circuitry allowing use at higher frequencies. Since the chip is back-to-back it has symmetric C/V characteristics. The group reported a peak output power of 198 μW at 200 GHz and a peak efficiency of 3.3 % which is comparatively low when considering Schottky diode performance at the same frequency.

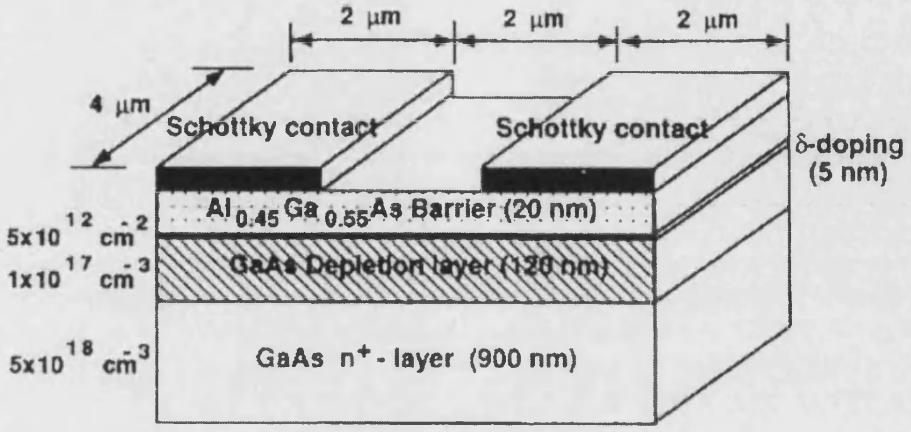


Fig. 3.18 Schematic of the back-to-back BNN varactor chip [3.19].

Another interesting novel nonlinear device is the metal/2-DEG (2-Dimensional Electron Gas). The 2-DEG was first introduced as the active element to multipliers in 1992 [3.20]. A Schottky contact is made at the edge of a 2-DEG as shown in Fig. 3.19. A strong nonlinear reactance can be observed in the area between the contact and the 2-DEG on application of a reverse bias. These devices show some advantages in efficiency and output power. They are also planar, so easily integrated into tiny multiplier systems and they tend to have high cut-off frequencies compared to GaAs devices. Koh *et al.* [3.21] achieved 0.62 mW peak output power and 1.24 % peak efficiency with their tripler to 225 GHz. Again, this structure did not perform as well as the GaAs structures although has some key advantages.

With planar technology now being introduced into many aspects of the fabrication process, researchers tended to move away from the conventional coaxial filters to multi-element distributed stripline filters. In a paper by Thornton *et al.* [3.22] the gradual transition from conventional to planar technology can be seen. A type of whisker contact was used to the diode, but the whisker was lithographically formed as part of the substrate and integrated filter. Here they demonstrated a double whisker formed using planar lithographic techniques so two diodes could be

contacted simultaneously. Suspended microstrip filters were implemented but no integration of the diodes into the substrate was seen yet. However they achieved 15 mW output power and 5 % efficiency at 271 GHz.

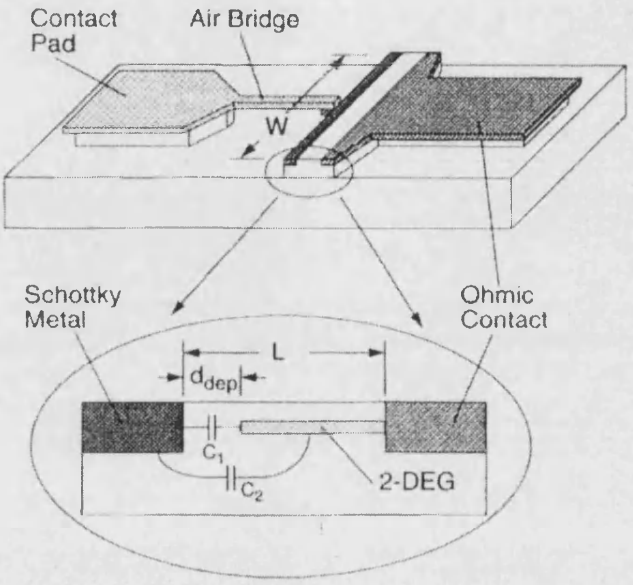


Fig. 3.19 Diagram of the metal/2-DEG Schottky device. Device is 100 μm wide (W) device length is shown (L), d_{dep} is the length of the depleted 2-DEG, C_1 represents the equivalent parallel plate capacitance and C_2 represents capacitance analogous to two coplanar strips [3.21].

The next landmark in multiplier development came in 1998 in two papers by Porterfield. The first [3.23] described in-depth modelling of a doubler to 80 GHz with impressive output power and efficiency. The second paper [3.24] evaluated the doubler in more detail. The doubler had six diodes in a 2 x 3 anti-series balanced configuration placed across a reduced height input waveguide. Input and output waveguides were crossed but in the same plane with a fixed output backshort and connected via a small cavity as shown in Fig. 3.20. The diode chip, made at the university of Virginia, was wire bonded across a quartz substrate which had a lithographically formed metal microstrip patterns for filters, transmission lines and output antenna. Harmonic balance analysis (explained in Chapter 6), using a program written by Siegel and Kerr [3.15], was used in conjunction with a microwave design system to optimize embedding impedance. Positioning of the diodes in the input waveguide along with microstrip tuning stubs and impedance transformers were also implemented in the optimized design. Due to the balanced configuration there was no need for this doubler to have a filter between input and

output waveguide. By reducing the input waveguide height, modes at the output frequency were not supported by the input waveguide and hence output frequency was restricted to the output circuit. Although only doubling to 80 GHz the multiplier had a peak output power at 96 mW (175 mW when cooled to 41K) and 48 % efficiency along with a 17 % 3 dB bandwidth. Fig. 3.21 shows power output as a function of frequency for 12 and 13 um diameter diode anodes.

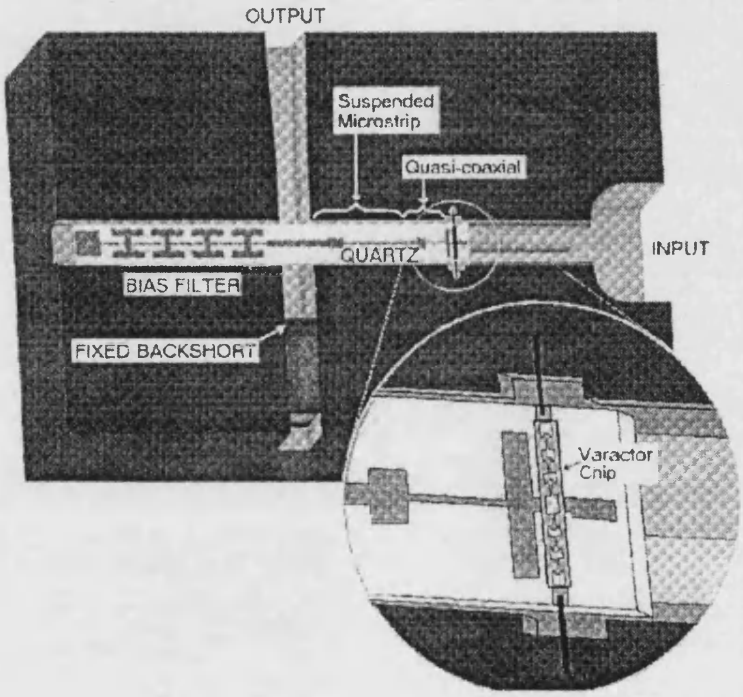


Fig. 3.20 40/80 GHz planar balanced frequency doubler showing close up of varactor chip [3.24].

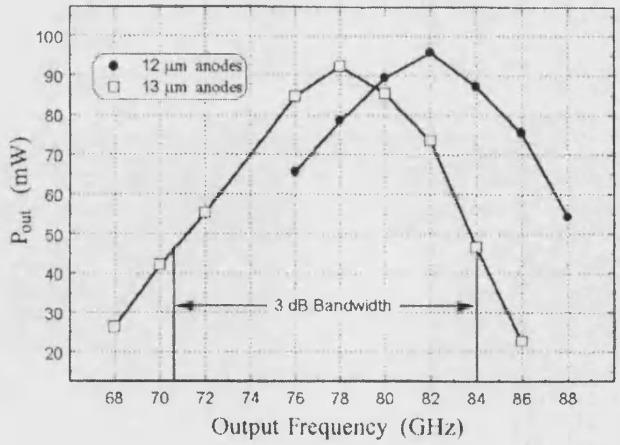


Fig. 3.21 Measured output power as a function of output frequency for 12 and 13 um diameter varactor anodes showing a 3-dB bandwidth for an input power level of 200 mW [3.24].

Very similar in design are two doublers reported by Newman and Erickson [3.25], illustrated in Fig. 3.22. The doublers both have a varactor array of 4 anodes and the rest of the structure is almost identical to that of Porterfield [3.24]. The first doubler output up to 50 mW in power at 160 GHz with peak 25 % efficiency. The second doubler output around 7 mW of power with a peak 31 % efficiency at 300 GHz. When cascaded together the quadrupler gave 6.1 mW peak output power and 7.2 % efficiency at 300 GHz.

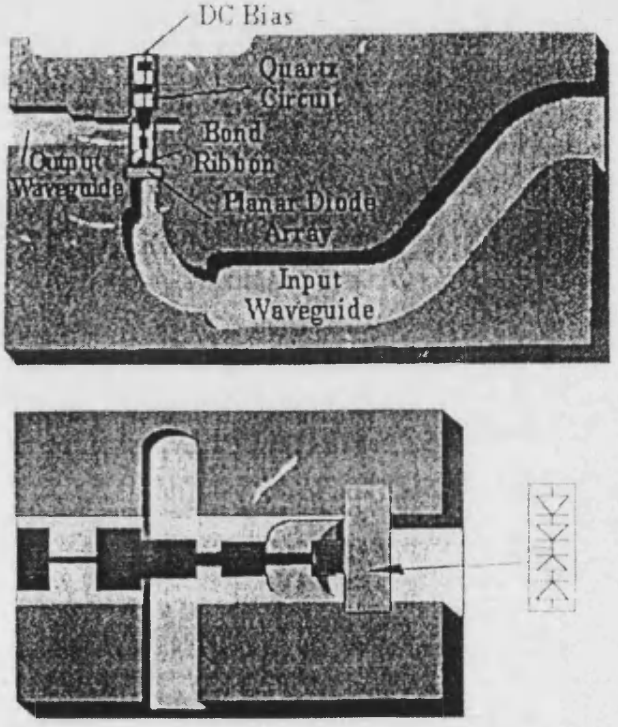


Fig. 3.22 Cross section of 160 GHz doubler showing positioning of 4 varactor diode chip in input waveguide [3.25].

The final part of this review is concerned with state-of-the-art multipliers in terms of their performance, achieved frequencies and the semiconductor processing technology used. Not only will an overview of current high frequency multipliers be given, but new fabrication techniques, processes and device structures that were used in the fabrication of the multiplier in this project. Some highly advanced modelling and fabrication methods will also be discussed involving equipment not available at the University of Bath but acknowledgement of this technology and its applications is considered.

Although highly advanced in both design and performance the Porterfield design [3.24] has one major drawback in its construction. The diode chip that is fabricated separately from the substrate needs to be bonded securely and with precision. When considering the size of the semiconductor chip (800 x 90 x 75 μm) and the accuracy needed in its positioning, it is obvious this is no simple task. The conventional method is called *flip-chip-bonding* and is a skilled art. The process involves heat to securely solder the chip in place which can damage the fragile electro-sensitive devices and the circuit also encounters some additional series resistance.

A method to overcome the flip-chip-bonding is to create the substrate out of the semiconducting material. This way the diodes do not need to be soldered into place and can be accurately positioned using lithographic techniques and connected to the rest of the circuit with lithographically formed microstrip transmission lines which can include filters. The process has now become completely planar, i.e. diodes, filters and microstrip transmission lines can all be formed on the semiconductor chip using one photolithographic mask. This planar process also has the advantage of producing multiple circuits simultaneously giving higher yields than, say, whisker contacted devices.

Introducing this method has brought about another problem. The additional GaAs increases the parasitic capacitance in the circuit which means to a high frequency RF signal the extra material causes extra loss. Obviously it is a general requirement that the passive part of the multiplier circuit is as loss-less as possible. However, by use of selective wet etching and dry reactive ion etching (RIE) the amount of lossy GaAs present in the multiplier circuit and hence RF losses can be minimized.

Multiplier circuits made on substrate material that have been thinned down to 3 μm in thickness have been reported, [3.26, 3.27] and even multipliers supported just by beam leads reported in [3.26]. By reducing the dielectric loading by such great amounts extremely high frequencies can be attained. Martin *et al.* [3.26] describe fabrication processes resulting in thin GaAs membranes and bare metal membranes. They report techniques to produce multipliers up to 800 GHz. They recommend not to use extremely thin membranes to aid heat dissipation in the diodes. The GaAs

layer structure is a standard n (0.2 μm), n^+ (1.5 μm) and AlGaAs etch stop layer (50 nm) with a semi-insulating substrate. The device process is shown in Fig. 3.23 where (a) shows definition of the mesa, which has the ohmic contact on, using RIE with BCl_3, SF_6 and Ar, (b) Schottky contacts made and air bridge metal deposited, (c) front side mounting in wax then backside thinning down to appropriate membrane thickness and device separation, (d) separated devices ready for mounting inside multiplier mount. An SEM of a completed 400 GHz doubler can be seen in Fig. 3.24 and the corresponding output response in Fig. 3.25. A higher frequency (up to 2.7 THz) process is described similar to the one above where a metal frame is developed around the device to support it in the guide. The 2.7 THz frequency tripler has a power output in the region of 0.1 μW, [3.28] which falls just short of the power requirement to run superconducting SIS or HEB mixers.

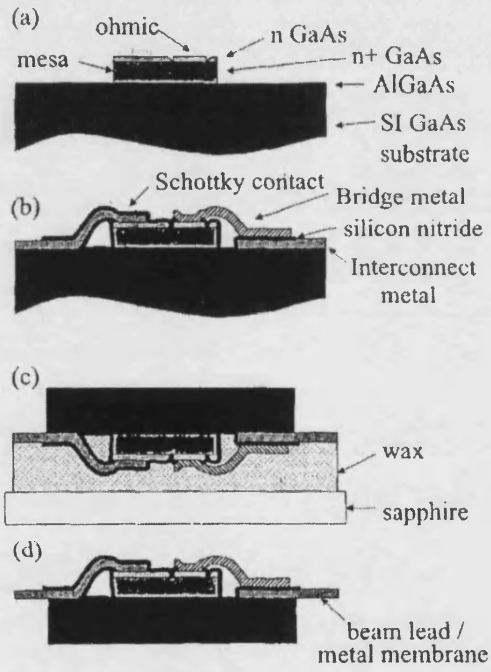


Fig. 3.23 Fabrication process steps to realize thin membrane structure (a) ohmic and mesa formation (b) Schottky contacts, interconnect metal and air bridge formation (c) backside thinning and device separation (d) release from carrier wafer [3.26].

Chattopadhyay *et al.* [3.29] developed a broadband balanced doubler to 800 GHz. This design was very similar to the design in this project. The multiplier had two Schottky diodes spanning the input waveguide in a balanced configuration on a 12 μm thick GaAs substrate. The diodes were earthed to the side of the guide and a free standing metal transmission line transmitted the second harmonic to the output

waveguide. No filters are used but an integrated silicon nitride (Si_3Ni_4) capacitor is used as an RF short and a DC bypass, shown on the RHS of Fig. 3.26. Again having an anti-series diode configuration suppressed all odd harmonics and again reduced input guide height restricted output frequency signals to the output circuit. The design is elegant and simple and the various electrical properties greatly reduce design and processing labour. The group reported 1.1 mW at 765 GHz and a peak 10 % efficiency.

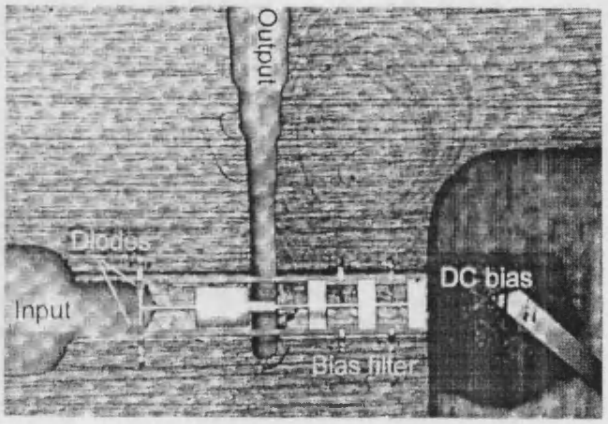


Fig. 3.24 400 GHz frequency doubler chip. Diodes are mounted on LHS of the chip and the output antenna is visible spanning the output waveguide of this novel substrateless design [3.28].

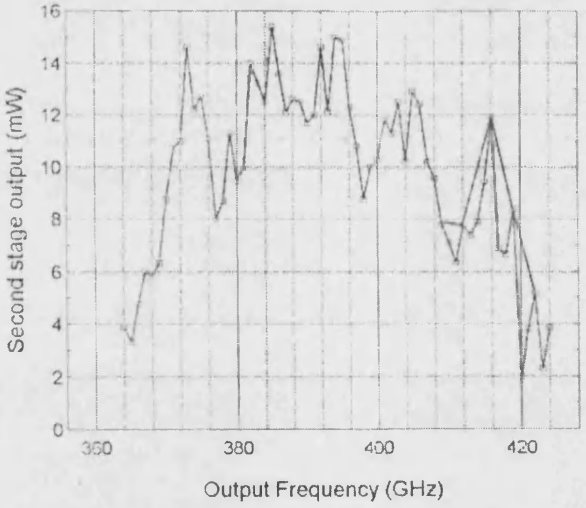


Fig. 3.25 Output of 400 GHz doubler at 80 K [3.28]

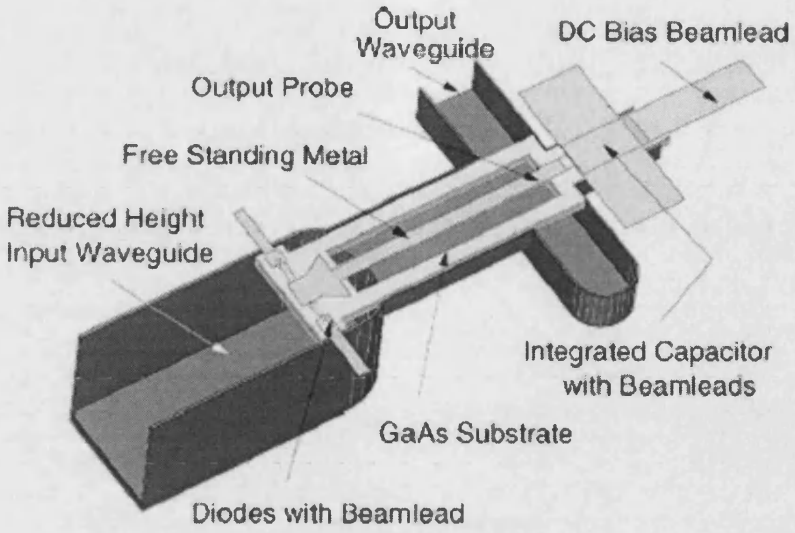


Fig. 3.26 Sketch of 800 GHz doubler showing chip supported in input waveguide by beam leads in the split block mount. The diodes are reverse biased and are biased through the bias beam lead, [3.30].

3.2 Summary

This section will condense and summarise the main trends described above. Many different multipliers of different orders using differing quantities of different types of diodes have been discussed in the review. Fig. 3.27 illustrates the general trend seen in this review of the output power as a function of frequency. The frequency denotes either the principle output frequency or the median of the output spectrum. The output power in each case is the peak output power reported and so this graph gives only a rough impression. The graph shows a basic trend, the higher the frequency the lower the attainable power. This trend is due to the higher losses inherently associated with higher frequency RF systems. Fig. 3.27 also differentiates between multipliers using single diodes, a balanced pair and HBV or QBV diodes. It is clear that the technology for HBV and QVB diodes is far from that of standard Schottky devices resulting in multipliers with poorer performance. Furthermore, multipliers using a balanced diode configuration seem to attain the highest power outputs. The second graph shown in Fig. 3.28 is an attempt to show the progress of multiplier development over the last 30 years. The graph indicators are split into four separate markers to indicate four different bands of frequency; 0 – 99 GHz, 100 – 199 GHz, 200 – 299 GHz, 300 – 399 GHz. This is done to show that in each frequency band

described there is a definite trend of improvement in output power of frequency multipliers over the last 30 years. It can be seen from Fig. 3.28 that improvements in technology and device processing over the years have lead to significant increases in output power levels in frequency multipliers along with pushing the boundaries of frequency up.

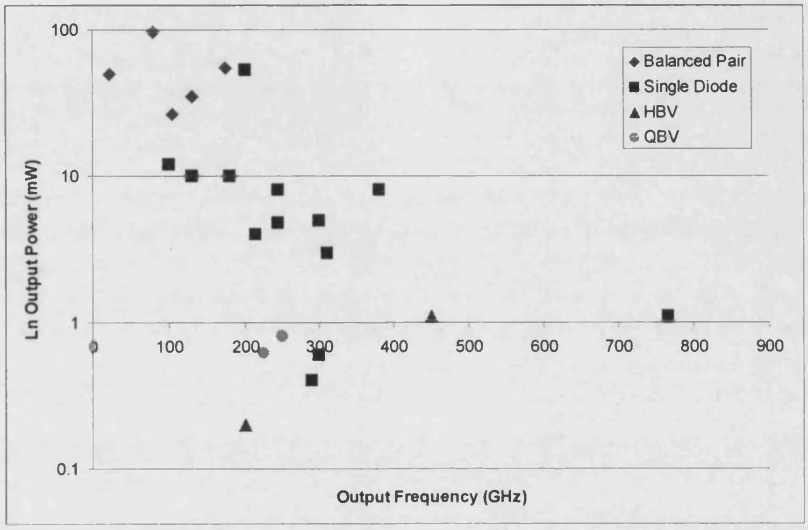


Fig. 3.27 Trend of output power as a function of output frequency for the variety of multipliers discussed in this review.

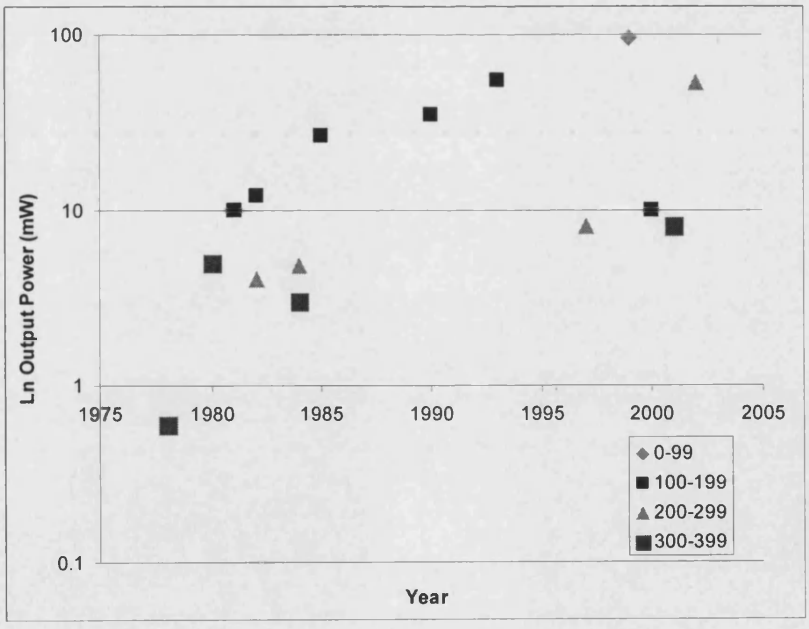


Fig. 3.28 Showing the evolution of multiplier development over the past 30 years by a gradual increase in output power with respect to frequency.

Chapter 3 – References

[3.1] R. P. Rafuse, D. Steinbrecher, "A 22-Gc balanced, canonically-tuned varactor quadrupler with 50-mW output power," *International Solid-State Circuits Conference*, 19th February, 1964, pp. 22-23.

[3.2] L. Cohen, *et al.*, "Varactor frequency doublers and triplers for the 200 to 300 GHz range," *Proc. IEEE MTT-S Int.*, 14-7 1100, 1975, pp. 274-276.

[3.3] M. Hirayama *et al.*, "Submillimeter wave frequency multipliers and IMPATT oscillators," *Microwave Symp. Digest MTT-S Int.*, vol. 78, issue 1, June 1978, pp. 435-437.

[3.4] T. Takada, M. Ohmori, "Frequency triplers and quadruplers with GaAs Schottky-barrier diodes at 450 and 600 GHz," *IEEE Trans. on Microwave Theory and Techniques*, vol. MTT-27, no. 5, May 1979, pp. 519-523.

[3.5] T. Takada, *et al.*, "Hybrid integrated frequency doublers and triplers to 300 and 450 GHz," *IEEE Trans. on Microwave Theory and Techniques*, vol. MTT-28, no. 9, September 1980, pp. 966-973.

[3.6] J. W. Archer, "Millimeter wavelength frequency multipliers," *IEEE Trans. on Microwave Theory and Techniques*, vol. MTT-29, no. 6, June 1981, pp. 552-556.

[3.7] J. W. Archer, "A high performance frequency doubler for 80 – 120 GHz," *IEEE Trans. on Microwave Theory and Techniques*, vol. MTT-30, no. 5, June 1982, pp. 824-825.

[3.8] N. R. Erickson, "A high efficiency frequency tripler for 230 GHz," *Proceedings of the 12th European Microwave Conference*, Helsinki, Finland, September 1982, pp. 228-292.

[3.9] J. W. Archer, "An efficient 200 – 290 GHz frequency tripler incorporating a novel stripline structure," *IEEE Trans. on Microwave Theory and Techniques*, vol. 32, no. 4, April 1984, pp. 416-420.

[3.10] J. W. Archer, "A novel quasi-optical frequency multiplier design for millimeter and submillimeter wavelengths," *IEEE Trans. on Microwave Theory and Techniques*, vol. 32, no. 4, April 1984, pp. 421-427.

[3.11] J. W. Archer, M. T. Faber, "High-output, single- and dual-diode, millimeter-wave frequency doublers," *IEEE Trans. on Microwave Theory and Techniques*, vol. MTT-33, no. 6, June 1985, pp. 533-538.

[3.12] A. Rydberg, H. Gronqvist, "Quantum-well high-efficiency millimeter-wave frequency tripler," *Electronics Letters*, vol. 25, no. 5, March 1989, pp. 348-349.

[3.13] T. Tolmunen, *et al.*, "High order frequency multipliers – a solution for mm- and submm-wave local oscillator signal generation," *IEEE MTT-S Digest*, vol. PP-28, 1989, pp. 1223-1226

[3.14] N. Erickson, "High efficiency submillimeter frequency multipliers," *IEEE MTT-S Digest*, vol. PP-1, 1990, pp. 1301-1304.

[3.15] P. Siegel *et al.*, "Topics in the optimization of millimeter-wave mixers," *NASA Technical Paper*, 2287, 1984.

[3.16] A. Rydberg, *et al.*, "Millimeter- and submillimeter-wave multipliers using Quantum-Barrier-Varactors (QBV) diodes," *IEEE Electronic Device Letters*, vol. 11, no. 9, September 1990, pp. 373-375

[3.17] S. Hollung, *et al.*, "A distributed heterostructure barrier varactor frequency tripler," *IEEE Microwave and Guided Wave Letters*, vol. 10, no. 1, January 2000, pp. 24-26.

[3.18] B. J. Rizzi, T. W. Crowe, N. R. Erickson, "A high power millimeter-wave frequency doubler using a planar diode array," *IEEE Microwave and Guided Wave Letters*, vol. 3, no. 6, June 1993, pp. 188-190.

[3.19] D. Choudhury, *et al.*, "Experimental performance of a back-to-back barrier-N-N^+ varactor tripler at 200 GHz," *IEEE Trans. on Microwave Theory and Techniques*, vol. 42, no. 4, April 1994, pp. 755-758.

[3.20] W. C. B. Peatman, *et al.*, "A novel Schottky/2-DEG diode for millimeter and submillimeter wave applications," *IEEE Electronic Device Lett.*, vol. 13, no. 1, January 1992, pp. 11-13.

[3.21] P. J. Koh, *et al.*, "Millimeter wave tripler evaluation of a metal/2-DEG Schottky diode varactor," *IEEE Microwave and Guided Wave Lett.*, vol. 5, no. 2. March 1995, pp.73-75.

[3.22] J. Thornton, *et al.*, "A high power 270 GHz frequency tripler featuring a Schottky diode parallel pair," *IEEE MTT-S Digest*, vol. WE3F-54, 1997, pp. 957-958.

[3.23] D. W. Porterfield, *et al.*, "An 80/160 GHz broadband, fixed-tuned, balanced frequency doubler," *IEEE MTT-S Digest*, vol. WE1A-2, 1998, pp. 391-394.

[3.24] D. W. Porterfield, *et al.*, " A high-power fixed-tuned- millimeter-wave balanced frequency doubler," *IEEE Trans. on Microwave Theory and Techniques*, vol. 47, no. 4, April 1999, pp. 419-425.

[3.25] T. Newman, N. Erickson, "A planar varactor array multiplier chain to 300 GHz," *IEEE MTT-S Digest*, vol. MO2C-5, 1999, pp.135-138.

[3.26] S. Martin, *et al.*, "Fabrication of 200 to 2700 GHz multiplier devices using GaAs and metal membranes," *IEEE MTT-S Digest*, vol. TH2D-2, 2001, pp. 1641-1644.

[3.27] A. Maestrini, *et al.*, "Performance of a 1.2 THz frequency tripler using a GaAs frameless membrane monolithic circuit," *IEEE MTT-S*, vol. TH2D-2, 2001

[3.28] F. Maiwald, *et al.*, "2.7 THz waveguide frequency tripler using monolithic membrane diodes," *IEEE MTT-S Digest*, vol. TH2D-1, 2001, pp. 1637-1640.

[3.29] G. Chattopadhyay, *et al.* "A broadband 800 GHz Schottky balanced doubler," *IEEE Microwave and Wireless Components Letters*, vol. 12, no. 4, April 2002, pp. 117-118.

[3.30] G. Chattopadhyay, *et al.* "An all-solid-state broad-band frequency multiplier chain at 1500 GHz," *IEEE Trans. on Microwave Theory and Techniques*, vol. 25, no. 5, May 2004, pp. 1538-1547.

Chapter 4

Diode Theory & Modelling

For the multiplier to work efficiently its active device, the Schottky varactor diode, must perform within certain parameters. These parameters are defined through a basic understanding of the multiplier system and are tested under DC and RF conditions. A general rule, however, is that the device should have a low series resistance, a low *ideality*. For effective biasing it is also necessary for the diode to have a high reverse breakdown voltage and good, low resistance ohmic contacts.

The diode's impedance can be categorised into different components not just of the varactor contact but also the surrounding semiconductor and metal material. Some of these impedances can be highly frequency dependent and care must be taken when making diodes for high frequency applications.

Methods are discussed below on how to improve varactor performance in a multiplier such as optimising the diode anode geometry, the doping concentration of semiconductor layers and the thickness of those layers.

Of key importance was knowing the behaviour of the diode capacitance and the diode series resistance at key frequencies for this information was used in the harmonic balance analysis in Chapter 6 which formed the final part of the multiplier modelling.

4.1 Diode Theory

Some early work into diode behaviour, or metal-crystal interface behaviour as it was previously referred to, should be mentioned here. In 1847 Braun [4.1] reported observations of the directional behaviour of metal contacts on natural and artificial metallic sulphides. Braun noted the nonlinear I/V characteristics of the contact and its rectifying properties. Braun also suggested in meticulous detail an insightful hypothesis on the observations of the directionality of the current involving

expanding and contracting tetrahedral inside the crystal. In 1938 Schottky [4.2] described an early account of the depletion region between metals and semiconductors and the barrier that is formed between them. Schottky also described the 'free electrons in excess semiconductors' which are now referred to as electrons in *n* type materials and 'deficit electrons in deficit semiconductors' which are now referred to as holes in *p* type materials. Early work done by Mott [4.3] described the metal semiconductor interface in terms of energy band diagrams and included the effect of impurity atoms in a semiconductor. Mott also included analysis of e-h pair generation and complex mathematical analysis of carrier transport in semiconductors. Some good accounts of metal semiconductor interface behaviour are also described in [4.4], [4.5].

The energy band structure of a metal and an *n* type semiconductor are shown in Fig. 4.1. The electrons in the semiconductor have more energy than those in the metal. As a consequence when the two materials are put into contact the semiconductor loses electrons as they collect on the surface of the metal. In doing this the electrons leave positive ionised donors in the semiconductor material. This creates a barrier between the two materials. Theoretically, the continuity of the Fermi level means bending of the semiconductor valence and conduction bands and as a result a barrier is formed with potential $q\Phi_b$.

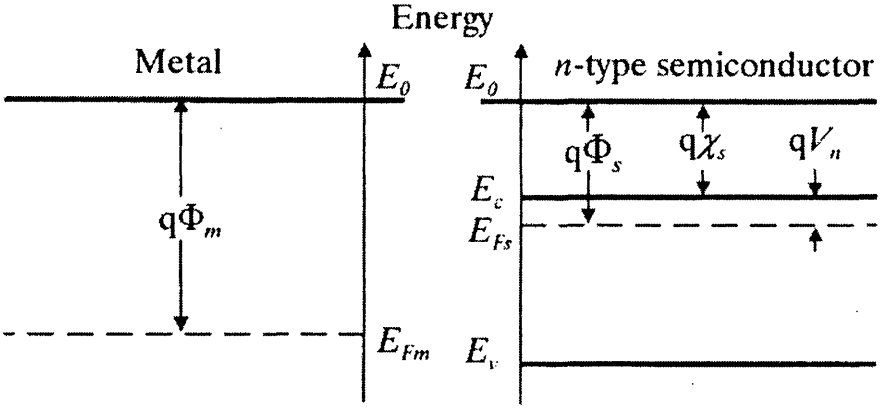


Fig. 4.1 Shows the band structure of a metal and semiconductor before intimate contact. Φ_m and Φ_s are the work functions of the metal and semiconductor respectively, E_{Fm} and E_{Fs} are the Fermi levels in the metal and semiconductor respectively, E_v and E_c are the energy levels of the valence and conduction bands respectively, χ_s is the electron affinity of the semiconductor, V_n is the difference between the semiconductor Fermi level and the conduction band and E_0 is the zero or vacuum level [4.6].

Fig. 4.2 illustrates the energy band of the metal-semiconductor interface when (a) in thermal equilibrium (b) when a forward bias voltage is applied and (c) when a reverse bias voltage is applied across the junction. Taking a physical perspective, the positive ions left behind in the semiconductor and the electrons at the surface of the metal form an electric field. This field is directly proportional to the amount of electrons that passed from semiconductor to the metal and this is generally determined by the specific materials used.

The barrier height is different for various metals but is always determined by [4.7]

$$\Phi_b = V_{bi} + V_n \tag{4.1}$$

where V_n is given by

$$V_n = \frac{kT}{q} \ln \frac{N_c}{N_D} \tag{4.2}$$

where k is the Boltzmann constant, T is the temperature, q is the charge on an electron, N_c is the density of states in the conduction band of the semiconductor (equal to 4.7 x 10^{17} cm^{-3} in GaAs at 300 K) and N_D is the doping density of the GaAs epilayer.

An example of barrier height for different metals on silicon and gallium arsenide is given in Fig. 4.3.

The depletion approximation assumes that no conduction electrons exist in the region denoted by bent energy bands ($0 < x < w$ in Fig. 4.2) and the resulting charge is due entirely to positive donor ions. The depletion region width, w, is given by [4.6]

$$w = \left[\frac{2\varepsilon_s}{qN_D} (V_{bi} - V_b) \right]^{1/2} \tag{4.3}$$

where ε_s is the total permittivity of the semiconductor, V_{bi} is the built-in potential and V_b is the applied bias voltage.

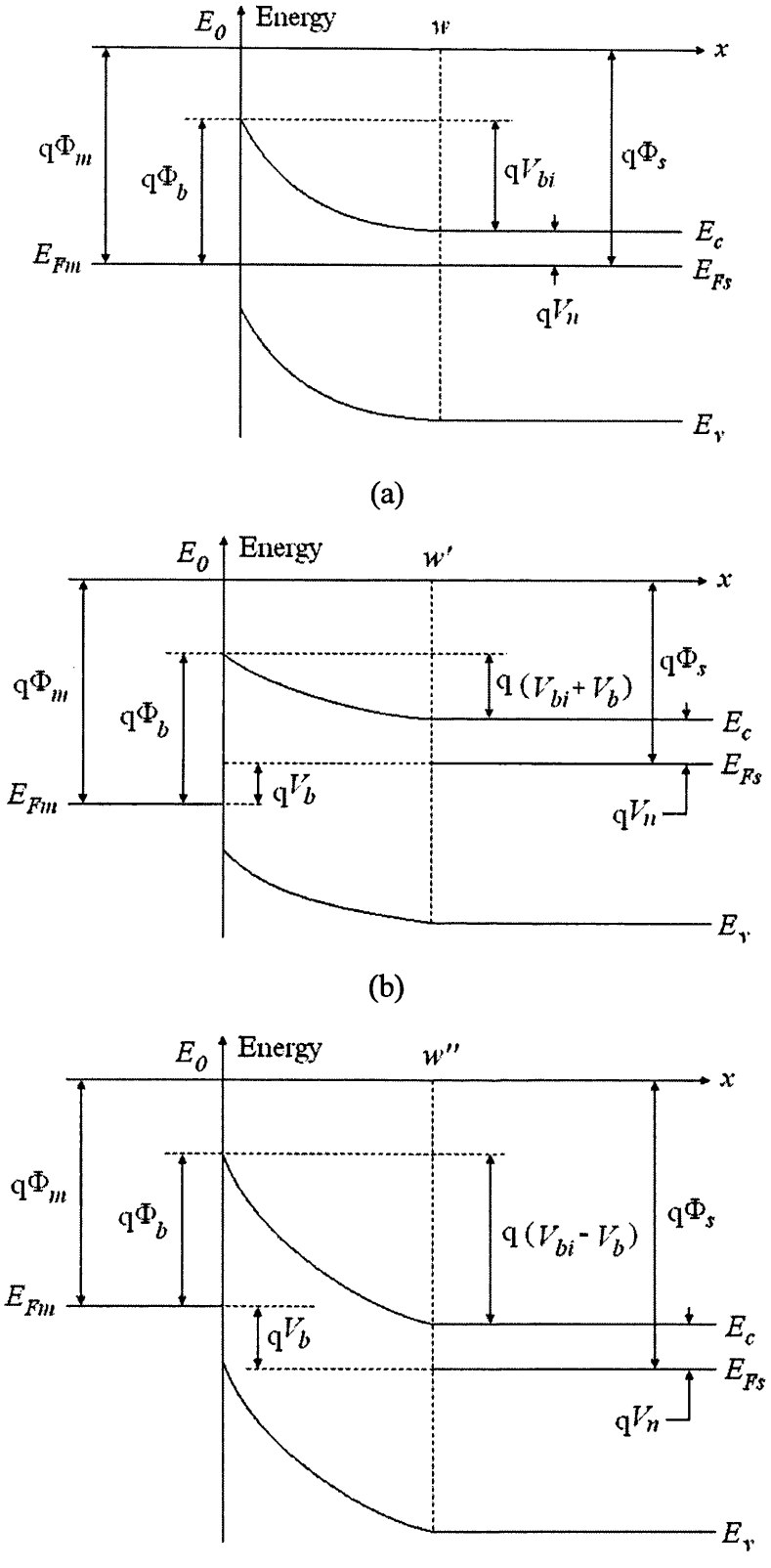


Fig. 4.2 Energy band diagram of metal and *n* type semiconductor in (a) thermal equilibrium (b) with an applied forwards bias voltage V_b and (c) with a reverse bias voltage V_b. Φ_b is the potential of the barrier and V_b is the external bias applied to the junction, V_{bi} is the built-in voltage and *w*, *w'* and *w''* is the depletion region width at equilibrium, with forward bias and with reverse bias.

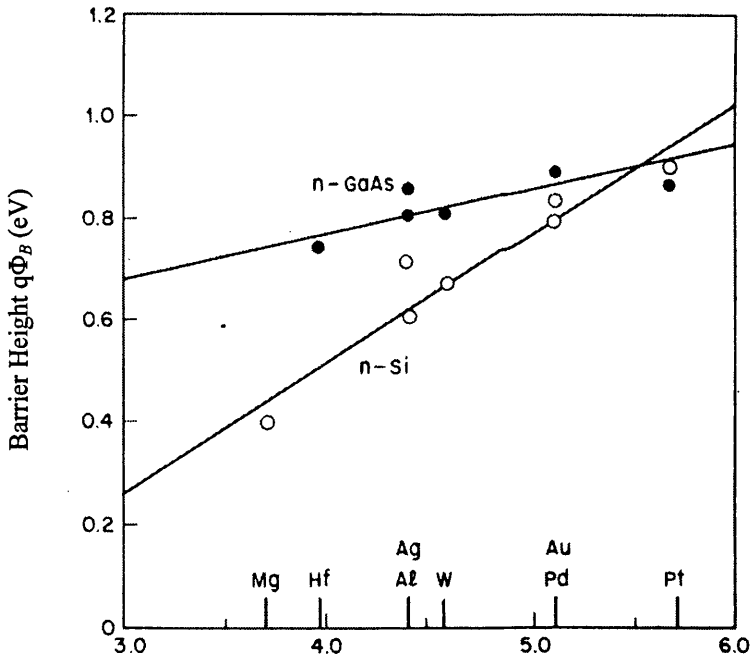


Fig. 4.3 Barrier height for metal-silicon and metal-gallium arsenide contacts, [4.7].

The diode junction capacitance C_j of an anode of area A_0 is therefore given by

$$C_j = A_0 \sqrt{\frac{q \varepsilon N_D}{2(V_{bi} - V_b)}} \tag{4.4}$$

which can be used to determine N_D , V_{bi} and hence Φ_b from a plot of $1/C_j^2$ versus V_b, (as used in section 7.2.2.5 and 8.1).

A more detailed analysis of the depletion layer shape is given in [4.8] where anode edge effects at high frequencies play an important role in the voltage modulation. The space charge per unit area from the ionised donors in the depletion region is given by

$$Q_{sc} = qN_D w. \tag{4.5}$$

By calculating the net charge of the depletion region the capacitance of the Schottky contact can be found [4.9]

$$C_j = \frac{\varepsilon_s A_0}{w}\left(1 + b\frac{w}{R_0}\right) \tag{4.6a}$$

where R_0 is the radius of the diode anode. The second term in the parentheses is a first order correction factor for frequencies corresponding to millimetre wavelength and b is a numerical constant equal to 1.5. At submillimetre wavelengths a second correction factor is added given by [4.10]

$$C_j = \frac{\varepsilon A_0}{w}\left(1 + b_1\frac{w}{R_0} + b_2\frac{w^2}{R_0^2}\right) = \frac{\varepsilon A_0}{w}\gamma_c \tag{4.6b}$$

where $b_1 = 1.5$ and $b_2 = 0.3$. The correction factor, γ_c, can vary typically from 1.0 ($w = 0$) to 1.5 ($w = t_e = R_0/3$) during a pump cycle. Equation (4.6b) was used in Section 6.3 for the nonlinear component of the junction capacitance in the harmonic balance analysis.

The theoretical energy band representation depicted in Fig. 4.2 is almost never attained due to the method in which the metal contact is made to the semiconductor. Usually a thin layer of oxide is formed on the surface of the semiconductor before the metal can be deposited. This usually means the barrier height is more dependent on the interface defects or surface states than the type of metal used. Gelmont *et al.* [4.11] extensively model the C/V characteristics of the Schottky junction including geometries other than small circles.

4.2 Diode Current Considerations

The ideality term mentioned in the introduction to this chapter refers to the type of current transport across the barrier. If a diode is to have perfect ideality ($\eta = 1.0$) the only transport mechanism for the carriers should be thermionic emission over the potential barrier. This is where carriers are given the energy to jump the barrier which is typically 0.8 eV for metal/ GaAs interface. Thermionic emission will only occur in low doped ($N_D << 10^{17}$ cm^{-3}) GaAs and with a relatively low bias voltages. Higher doped material and higher bias conditions lead to quantum-mechanical

tunnelling through the barrier. Any part of the current transported in this way will result in a departure from the perfect ideality ($\eta > 1.0$). Some researchers [4.12] have found it useful to lower the barrier height of the Schottky contact. This would mainly be used for mixers or detectors in the THz frequency range where only low drive levels are available.

4.2.1 Barrier Current Transport Mechanisms

4.2.1.1 Thermionic Emission

Two main theories exist over the process which sets the limit of current through emission over the barrier. *Diffusion theory* suggests the current is limited to drift and diffusion of carriers in the depletion region. *Thermionic-emission theory* suggests that the current is set by the rate of transfer of carriers from the semiconductor to the metal and that diffusion is negligible. Fig. 4.4 demonstrates the basic current mechanisms.

A synthesis of the two theories was formed by Crowell and Sze [4.7] suggesting a continuum of the two mechanisms. This meant that the current from drift and diffusion should equal that of the thermionic emission and as a result, at low bias conditions, the current across the junction should be

$$J_b = \left[A^{**}T^2 \exp\left(-\frac{q\Phi_b}{kT}\right)\right]\left[\exp\left(\frac{qV_b}{kT}\right)-1\right] \tag{4.7a}$$

$$J_b = J_s\left[\exp\left(\frac{qV_b}{kT}\right)-1\right] \tag{4.7b}$$

where A^{**} is the modified Richardson constant which, at moderate doping levels (10^{16} to 10^{17} cm^{-3}) and low bias, will be a constant value.

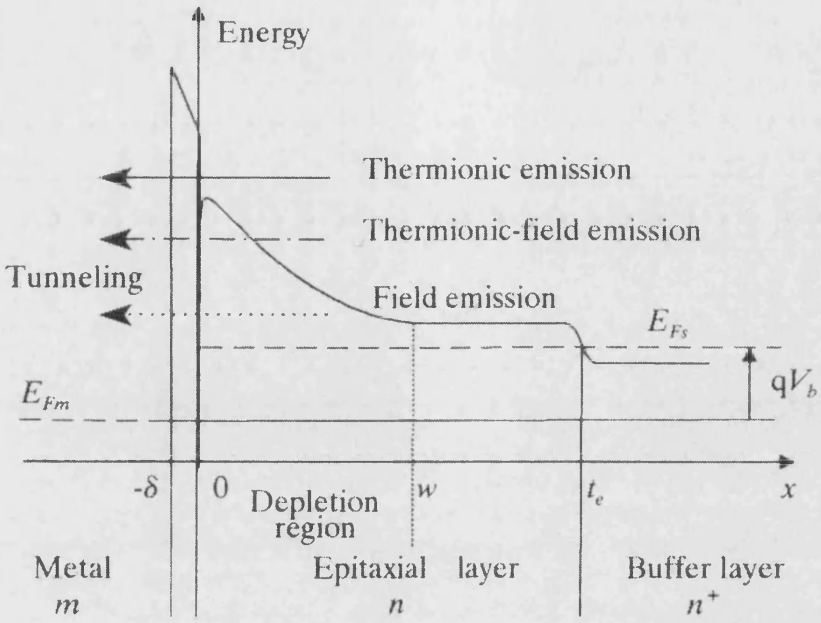


Fig. 4.4 Energy band diagram of a forward biased Schottky contact showing the main contributors to conduction across the barrier where t_e is the total epilayer thickness. The energy level spike between $-\delta < x < 0$ can arise from a non-perfect interface between the metal and the *n* layer of the semiconductor, e.g. presence of an oxide layer, [4.6].

The Richardson constant is a measure of the thermionic emission of carriers across the Schottky barrier. The modified Richardson constant accounts for quantum mechanical reflection and phonon scattering given by [4.13]. For GaAs the value is around 8.4 A cm^{-2} K^{-2} although this value will change with higher bias and or temperature, [4.6, 4.14].

4.2.1.2 Barrier Tunnelling

There are two main components to the tunnelling of carriers through the barrier [4.13, 4.15]. These occur at high doping densities and low temperature. *Field emission* occurs when the barrier is so thin, due to high doping and low temperature, that carriers may quantum-mechanically tunnel through the barrier. Alternatively, if the temperature is increased then the energy of the carrier is such that they see a very thin and much lower barrier and the probability of tunnelling is greatly increased. This is *thermionic-field emission* and is regulated by the fact that at higher temperatures only a small amount of carriers may hold this higher energy. This results in a temperature dependent balance between the two mechanisms. Obviously if the temperature is above a certain threshold then all carriers will have enough

energy to scale the barrier and the process becomes purely thermionic emission. Forward current density due to tunnelling is given by [4.16]

$$J_b = J_s \exp\left(\frac{V_b}{E_0}\right) \tag{4.8a}$$

where

$$E_0 = E_{00} \coth\left(\frac{qE_{00}}{kT}\right) \tag{4.8b}$$

and

$$E_{00} = \frac{h}{4\pi}\left(\frac{N_{De}}{m^* \varepsilon_s}\right)^{1/2}. \tag{4.8c}$$

J_b is the current density across the barrier, h is the Plank constant, $m^* = m_r m_o$ is the effective mass of the electrons in the n type semiconductor material and ε_s is the permittivity of the n type semiconductor material. J_s is the tunnelling saturation current which is a function of the temperature, barrier height and other semiconductor properties.

4.2.1.3 General I/V Characteristics and Ideality

The diodes used for frequency multiplying in this project had relatively low doping concentration for the active GaAs n layer, $N_D = 1.0 \times 10^{17}$ cm^{-3}, and operated at room temperature, 300 K, or below. This was sufficient to inhibit a tunnelling current through the barrier and therefore thermionic emission over the barrier dominated the current transport mechanism. However, the *ideality factor* was introduced to help describe the junction behaviour at various temperatures and doping levels and is given by [4.17]

$$\eta = \frac{q}{kT}\frac{\partial V_b}{\partial(\ln J_b)} \tag{4.9}$$

where an ideality of one indicates pure thermionic emission and any increase above one is a deviation from the ideal model. Therefore the I/ V characteristic can be defined as

$$I_b = I_0\left[\exp\left(\frac{qV_b}{\eta kT}\right)-1\right] \tag{4.10}$$

where I_0 is the saturation current given by

$$I_0 = A_0 A^{**} T^2 \exp\left(-\frac{q\Phi_b}{kT}\right). \tag{4.11}$$

Equations (4.10 & 4.11) were used in sections 7.2.2.5 and 8.1 to determine the saturation current and hence barrier height from I/V measurements on actual diodes (an alternative to using (4.4) from diode C/V measurements).

4.2.2 Ohmic Contacts

Ohmic contacts form the other half of the varactor diode, the cathode. Ideally fabricated they should pass current unimpeded from an external contact and into the highly doped (1.0×10^{18} cm^{-3}) n^+ layer of the semiconductor. Conventionally a gold/ germanium alloy is formed in a recess in the n^+ layer and capped with a refractory metal, e.g. titanium, which acts as a barrier during the high temperature alloying process [4.18]. The process is usually finished with a coating of a good contacting material such as gold. This process is obviously needed as placing a metal in contact with a highly doped semiconductor will still result in a Schottky contact.

However, there is a certain degree of skill needed to attaining a perfect ohmic contact and as a result they do have a finite resistance which can affect multiplier performance. One method to calculate this resistance is to consider the model in Fig. 4.5 where a planar ohmic contact sits on a material of resistivity ρ and the ohmic contact is characterised by the by the specific contact resistance r_c.

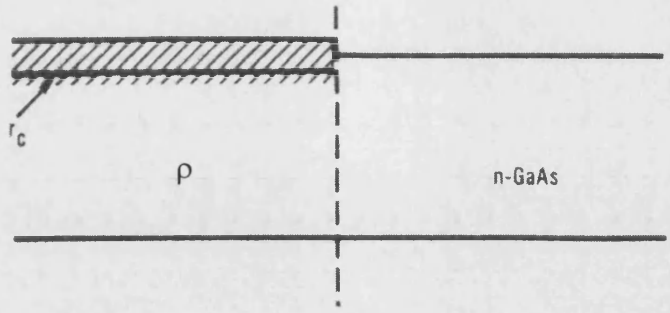


Fig. 4.5 Model of a planar ohmic contact, [4.19]

Following an equivalent circuit approach given in [4.19] the contact resistance is given by

$$R_c = \frac{\sqrt{R_{sh} r_c}}{W} \coth\left(\frac{d}{L_t}\right) \tag{4.12}$$

where R_{sh} is the sheet resistance of the semiconductor, W is the width of the contact, d is the length of the contact and L_t is the transfer length.

Another approach is to assume that the high doping levels will promote a dominantly tunnelling carrier transport mechanism. Therefore from

$$R_c \equiv \left(\frac{\partial J}{\partial V}\right) \tag{4.13}$$

and using equation (4.8) it follows that

$$R_c = \exp\left[\frac{4\pi\sqrt{m^*\varepsilon_s}}{h}\left(\frac{\Phi_b}{\sqrt{N_{De}}}\right)\right]. \tag{4.14}$$

4.2.3 Current Saturation

A major limiting factor in semiconductor devices used at high frequencies is fundamentally due to the limiting speed of the electrons travelling in the

semiconductor. This can limit input power levels coupled into the diode and hence limit maximum output power of the multiplier. If the amount of power coupled into a diode results in a displacement current, i_d, through the undepleted semiconductor, carrier saturation will occur and any further increase in input power will result in no further increase in output power. Furthermore, driving the diode into or beyond saturation will result in adverse heating and further degradation of device performance. Displacement current through the depletion region in the diode is given by [4.20]

$$i_d = C_j \frac{dV_b}{dt} \tag{4.15}$$

where C_j is the junction capacitance. In the diode the displacement current has to match with the current through the undepleted semiconductor material, the electron conduction current, i_e, given by

$$i_e = A_0 n_e v_e q \tag{4.16}$$

where n_e is the electron density (for n doped GaAs $n_e = N_D$) and v_e is the electron velocity. In GaAs the velocity of electrons usually peaks around 2.2 x 10^7 cm s^{-1}, considerably more than Si as shown in Fig. 4.6. A saturation scenario can be considered when $i_d > I_0$ where

$$I_0 = i_{e,\max} = N_{De} v_{e,\max} q A_0 \tag{4.17}$$

where $i_{e,max}$ is the maximum current through the undepleted epilayer and $v_{e,max}$ is the maximum electron velocity for the material.

As previously stated in Chapter 2, it is desirable to produce as much power as possible from a multiplier and therefore current saturation effects should ideally be reduced. Fig. 4.7 shows the experimental and theoretical efficiencies of a frequency doubler as a function of input power (and hence i_e) indicating where, in a theory suggested in [4.20], the saturated and unsaturated current areas should be. It is clear

from Fig. 4.4 that if the diodes in a multiplier are operating with saturated current levels a drop in efficiency is observed. Theoretical efficiencies are also shown for diodes with different series resistance. This illustrates the critical requirement for a diode to have a low series resistance and justifies the time and labour spent in minimising this quantity during fabrication.

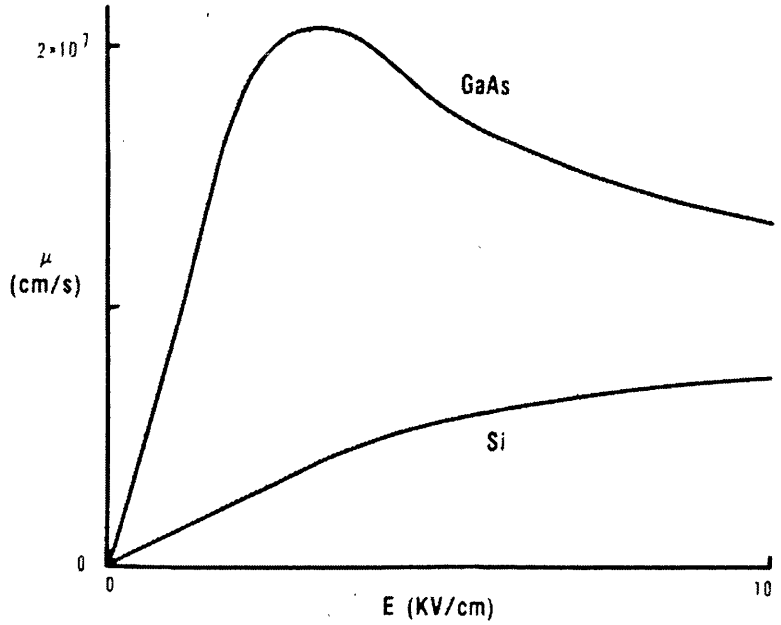


Fig.4.6 Drift velocity (μ) of electrons in GaAs and Si as a function of the electric field, GaAs being the obvious choice when considering high frequency applications, [4.19].

Increasing the doping concentration would not be a viable answer as this would affect the transport mechanism across the barrier. Increasing the diode area however, is certainly a credible candidate for increasing the saturation limit of the device. Consequently it is not viable to just use the largest area diodes as larger diodes have more parasitic losses. Therefore a balance must be found between current saturation, diode area and minimal parasitic capacitance. This trade-off is discussed in Chapter 6 where the varactor diode anode area is modelled as a function of multiplier performance.

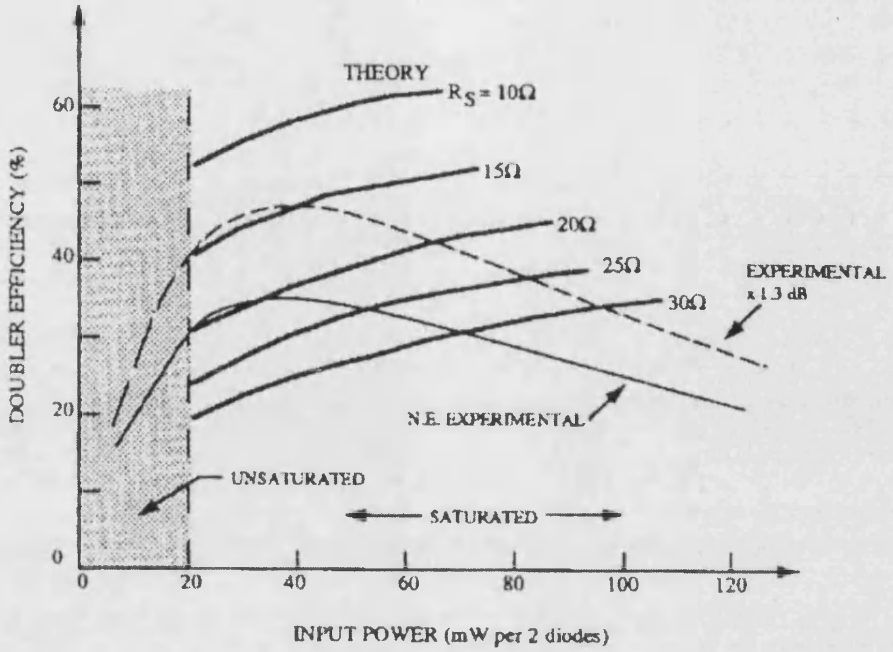


Fig. 4.7 Theoretical (heavy solid lines) [4.20] and experimental (solid: experimental, dashed: with 1.3 dB ohmic losses subtracted) [4.21] efficiencies for a frequency multiplier as a function of input power. Expected unsaturated region shown on LHS (shaded).

4.3 Impedance Considerations

This section will attempt to break down the components that make up the impedance of the Schottky diode from anode to ohmic contact. Nonlinear components, i.e. the voltage dependant capacitance given by (4.2) and (4.6) and the resistance associated with this will be dealt with separately in Chapter 6. Initially the undepleted epilayer impedance will be examined then spreading resistance, resistance of carriers travelling across the device surface and finally resistance to current flow to the cathode/ ohmic contact (previously introduced in (4.12) and (4.14)). Finally, parasitic losses not associated with the device directly but with the planar structure will be reviewed in the final subsection.

4.3.1 Undepleted Epilayer Impedance

The planar varactor diode structure is shown in Fig. 4.8, indicating the gold contact pad and finger (which contacts the anode), the ohmic contact, the insulating layer of silicon dioxide, the lightly doped active n layer, the higher doped n^+ layer and a semi-insulating substrate. Also shown is an etched air channel that isolates the

device during fabrication and reduces some of the parasitic losses explained later in this chapter and in Chapter 5.

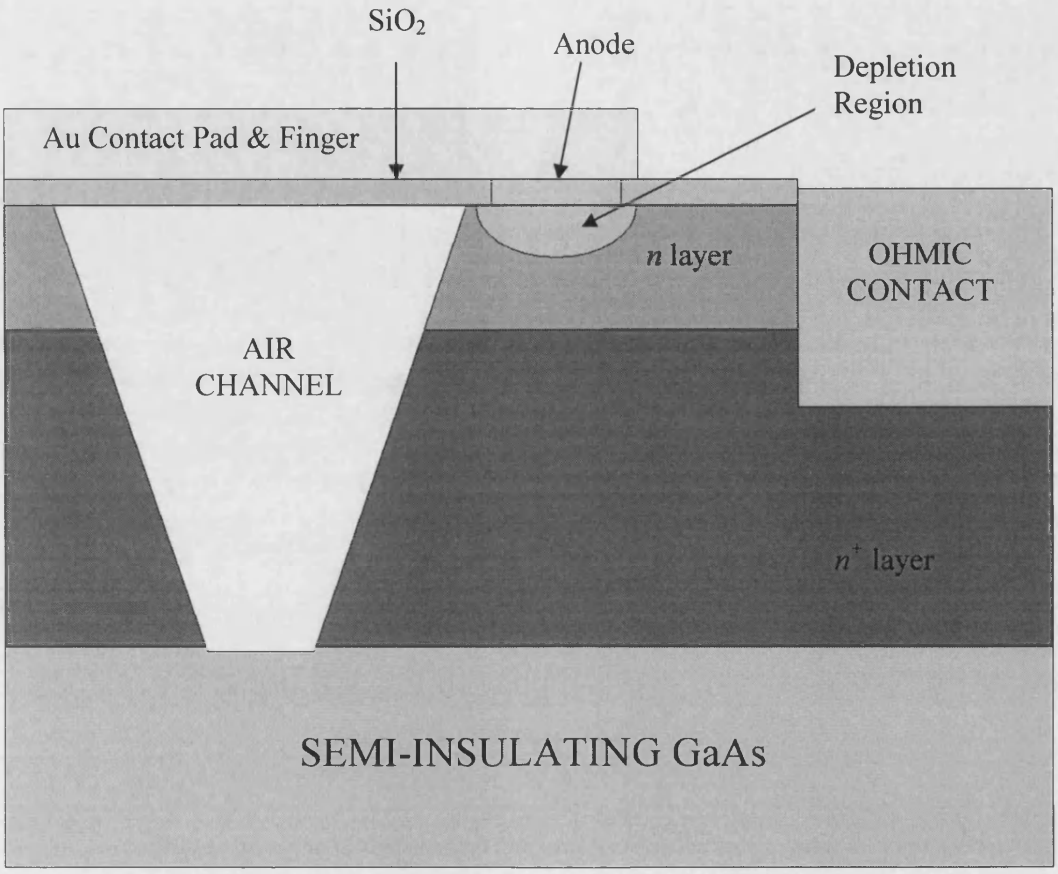


Fig. 4.8 Structure of a planar Schottky diode indicating: presence of SiO_2 to isolate contact pad and finger from the *n* layer, position of the air bridge to minimise parasitic capacitance, the anode and depletion region, ohmic contact and semi-insulating GaAs substrate.

Fig. 4.9 shows a close-up of the area directly under the anode and a simple equivalent circuit that describes its behaviour. The depletion region is equivalent to a nonlinear resistance in parallel with a nonlinear capacitance. As the varactor diodes are usually in high reverse bias R_j is usually very large and approximately constant when an RF signal is applied across the device. C_j, the nonlinear capacitance, is the most active part of the diode. When an external RF signal is applied the depletion region boundary will oscillate up and down resulting in the time dependent charge waveform (see Fig. 4.16).

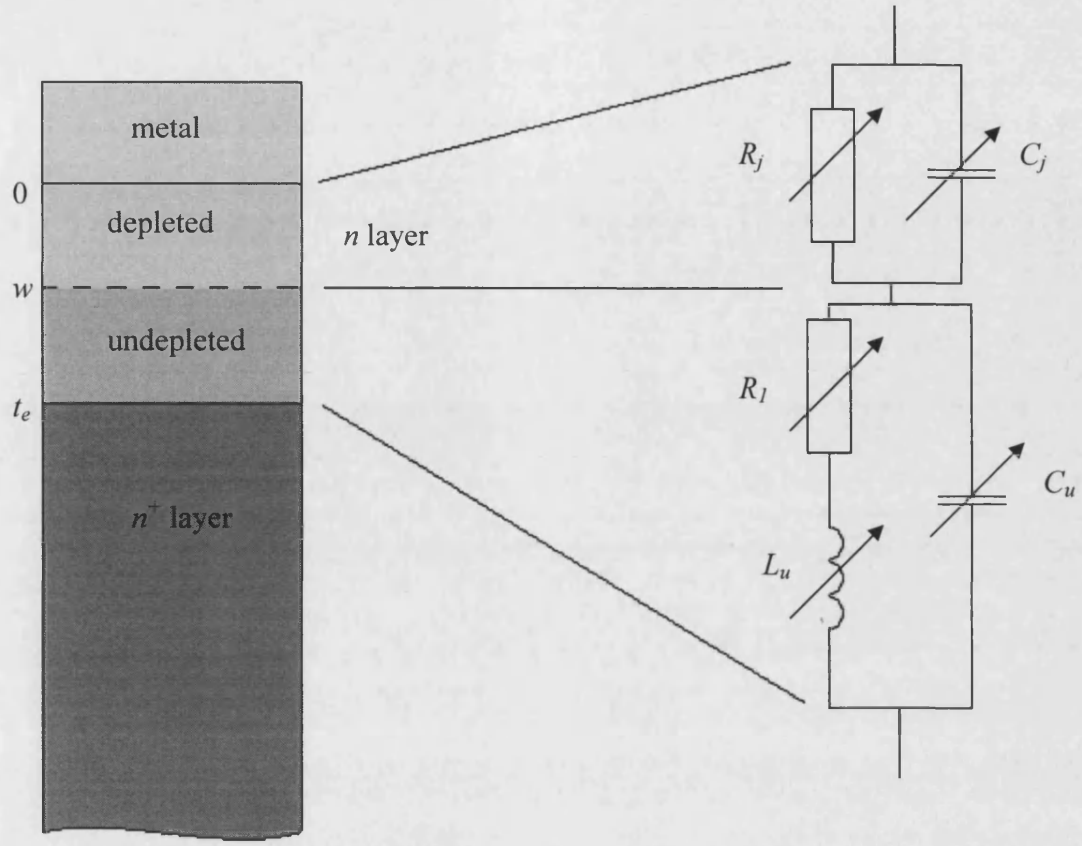


Fig. 4.9 Equivalent circuit of the Schottky contact. (LHS) layer structure: metal, lightly doped epilayer with depleted region from 0 to w and undepleted region w to t_e, n^+ layer represents the heavily doped layer. (RHS) Equivalent circuit of the relevant layer where R_j is the junction resistance, C_j is the junction capacitance, R_l, L_u and C_u are the undepleted epilayer resistance, inductance and capacitance respectively.

The diode series resistance in the multiplier can degrade performance dramatically with an increase of just 5 – 10 Ω, which is discussed in Chapter 6. It is therefore necessary to choose the layer structure of the device carefully. If the epilayer (n layer) is too thin, under high reverse bias the diode could *punch through* where the depletion region extends to the n^+ region. At this point no further capacitance modulation can occur and hence no multiplication would either. However, if the epilayer is chosen to be too thick this can increase the series resistance of the undepleted epilayer with no real improvement to the diode performance, i.e. breakdown voltage is not increased. Ideally diode breakdown under high reverse bias should occur at the edge of the depletion region which is ultimately determined by the doping concentration. Impedance of the undepleted epilayer, R_l Fig. 4.9, is given by [4.6]

$$R_1 = \frac{t_e - w}{A_0 q \mu_{e0} N_D} = \frac{(t_e - w)\rho_e}{A_0} \tag{4.18}$$

where t_e is the thickness of the epilayer, w is the width of the depletion region, A_0 is the area of the anode, μ_{e0} is the mobility of the electrons in the epilayer, N_D is the doping concentration in the epilayer and ρ_e is the resistivity in the epilayer.

Carriers in the undepleted region also display inertia effects due to nonzero effective mass which is modelled as inductance. Upon arrival at the potential barrier electrons travelling through the epilayer either pass over or are reflected similar to a scattering event. The transit time of electrons through this layer results in a scattering frequency $w_{s,eff}$. The inductance through the undepleted epilayer is given as

$$L_u = \frac{R_1}{\omega_{s,eff}} \tag{4.19}$$

where

$$\omega_{s,eff} = \frac{q}{m^* \mu_{e0}} + \frac{v_d}{t_e} \tag{4.20}$$

and v_d is the mean drift velocity of the electrons. A displacement current also accounts for a capacitance shunting the series undepleted epilayer resistance and inductance given by

$$C_u = \frac{\varepsilon_s A_0}{(t_e - w)}. \tag{4.21}$$

It is common to see this term omitted from most models. At frequencies below about 1 THz the reactance from C_u is much larger than the resistance from R_1 and therefore most of the current flows through the resistor. Therefore, unless at very high frequencies the displacement current is very small and can be neglected.

4.3.2 Resistance Through n^+ Layer

The flow of current as it passes into the higher doped n^+ layer can be further broken down into three main components. The first, R_2, is called the spreading resistance and is of paramount importance to diodes used in frequency multipliers. In varactor diodes used for harmonic multiplication, not only input and output signals will dissipate energy through the spreading resistance but also any idler frequencies. The spreading resistance is caused by high frequency signals being restricted to current flow in only the surface area of the semiconductor. The depth at which a high frequency signal penetrates a material is called the *skin depth* and is inversely proportional to frequency [4.22]

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{4.22}$$

where ω is the angular frequency, μ is the mobility of electrons in the material and σ is the conductivity of the material. Early work carried out on spreading resistance was reported by Dickens [4.22] and subsequently by McKinney [4.23] and Garfield [4.24].

Fig. 4.10 depicts the current paths from the anode to the cathode. R_1 has previously been discussed. R_2 is attributed to the spreading resistance and is given by [4.23]

$$R_2 = \frac{\rho_{n+}}{2\pi R_0}\tan^{-1}\left(\frac{\delta}{R_0}\right) + \frac{SF\rho_{n+}}{4\pi\delta} \tag{4.23}$$

where ρ_{n+} is the resistivity of the n^+ layer, R_0 is the anode radius and SF is a scaling factor to account for the current not taking a full radial pattern. The first half of (4.23) is resistance to current travelling vertically and the second half is resistance to current travelling towards the ohmic contact. The scaling factor, SF, is given by [4.25]

$$SF = \frac{360°}{2\phi + 180} \tag{4.24}$$

where ϕ is indicated in Fig. 4.11.

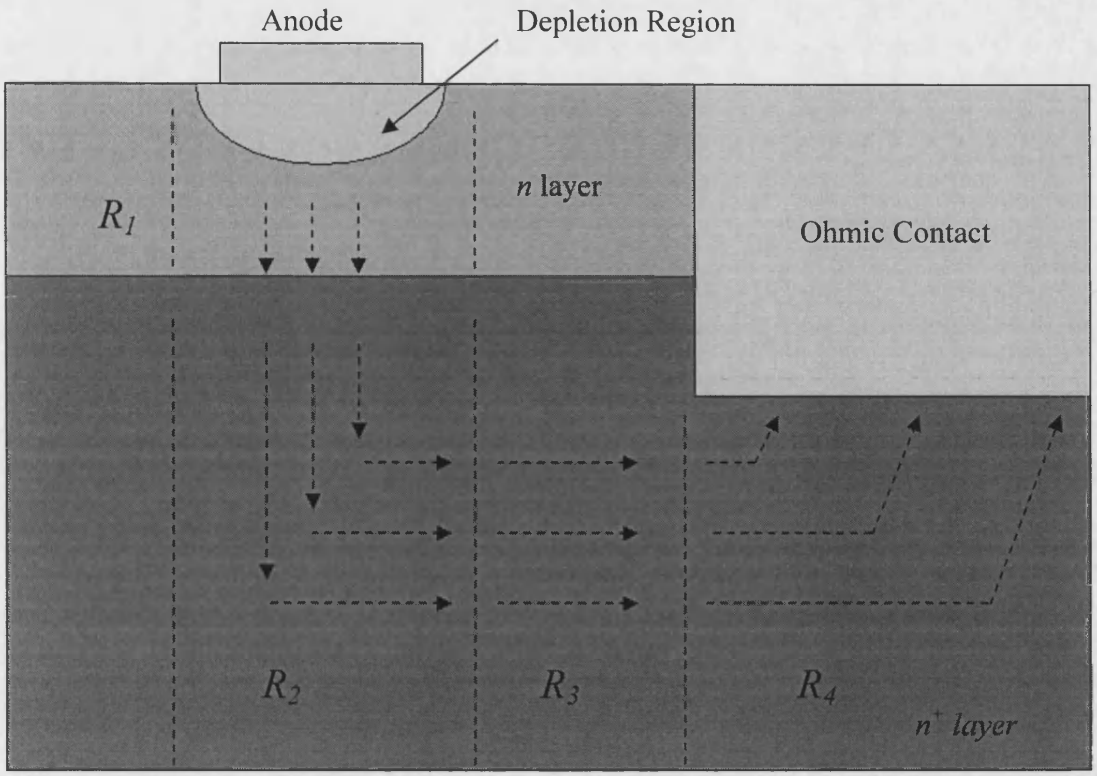


Fig. 4.10 The breakdown of series resistance through the n+ layer. R_2 is attributed to spreading resistance, R_3 is resistance to current flowing on the device surface and R_4 is resistance to current entering the ohmic contact.

R_3 is the contribution of the resistance due to current travelling on the surface of the n^+ layer and is given by Setzer as [4.26]

$$R_3 = \frac{\rho_{n+} SF}{2\pi\delta} \ln\left(\frac{r_x}{R_0}\right) \tag{4.25}$$

where r_x is the distance between the centre of the anode and the edge of the cathode. The final component is the resistance to current flowing into the ohmic, given by Setzer as [4.26]

$$R_4 = \frac{1}{SF\pi r_c}\left(\frac{\rho_n + r_c}{\delta}\right)^{1/2} \tag{4.26}$$

where r_e is the distance from the centre of the anode to the edge of the chip, ρ_n is the resistivity of the n layer and r_c is the specific contact resistance of the ohmic contact.

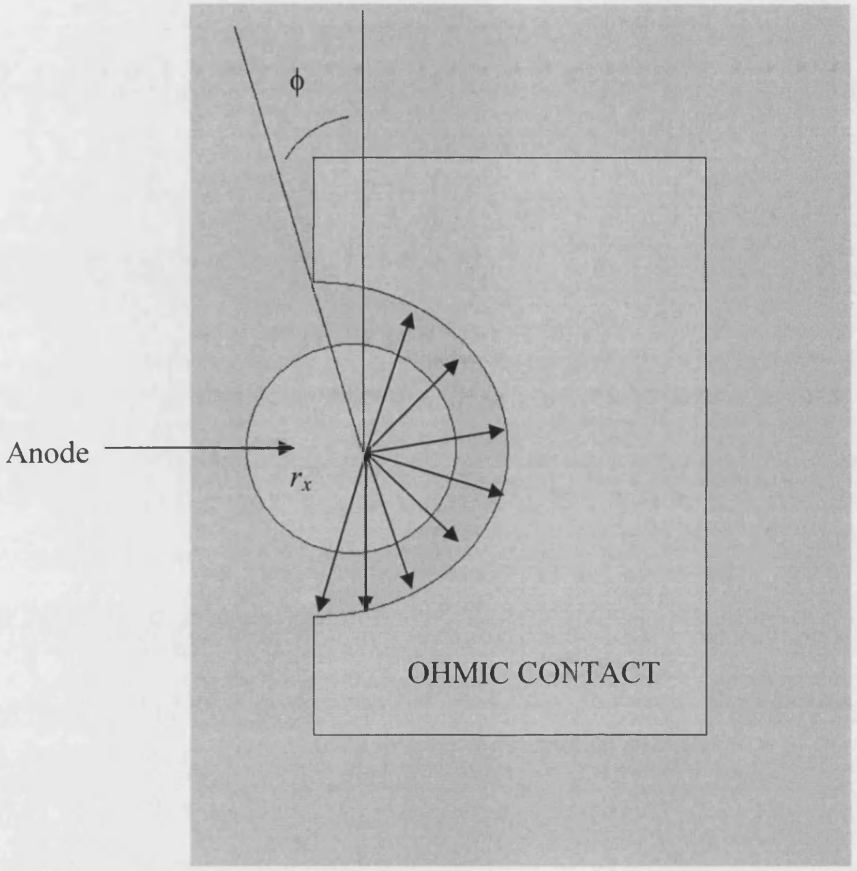


Fig. 4.11 Scaling factor used in calculating the spreading resistance.

4.3.3 Other Parasitic Losses

Compared to whisker contacted diodes, planar diodes have a number of inherent parasitic losses due to the overall structure. Although much more mechanically stable than whisker contacted diodes, planar diodes have the disadvantage of suffering from extra shunt capacitances as shown in Fig. 4.12.

Most of these extra capacitances were modelled during the structure simulation discussed in Chapter 5. However, some of these capacitances that cannot be considered as structure should be noted here and are illustrated in Fig. 4.13.

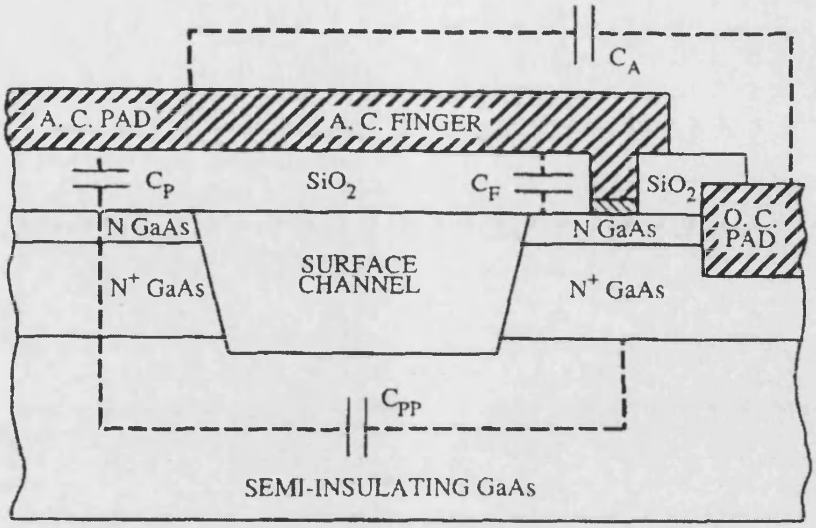


Fig. 4.12 Extra shunt capacitances: C_P is a parallel plate capacitance from the anode contact pad, C_F is a parallel plate capacitance due to the contact finger, C_A is the capacitance due to the fringing field above the chip from the anode contact pad and finger to the ohmic contact and C_{PP} is a relatively small fringing field component between the contact pads in series with C_P, [4.27].

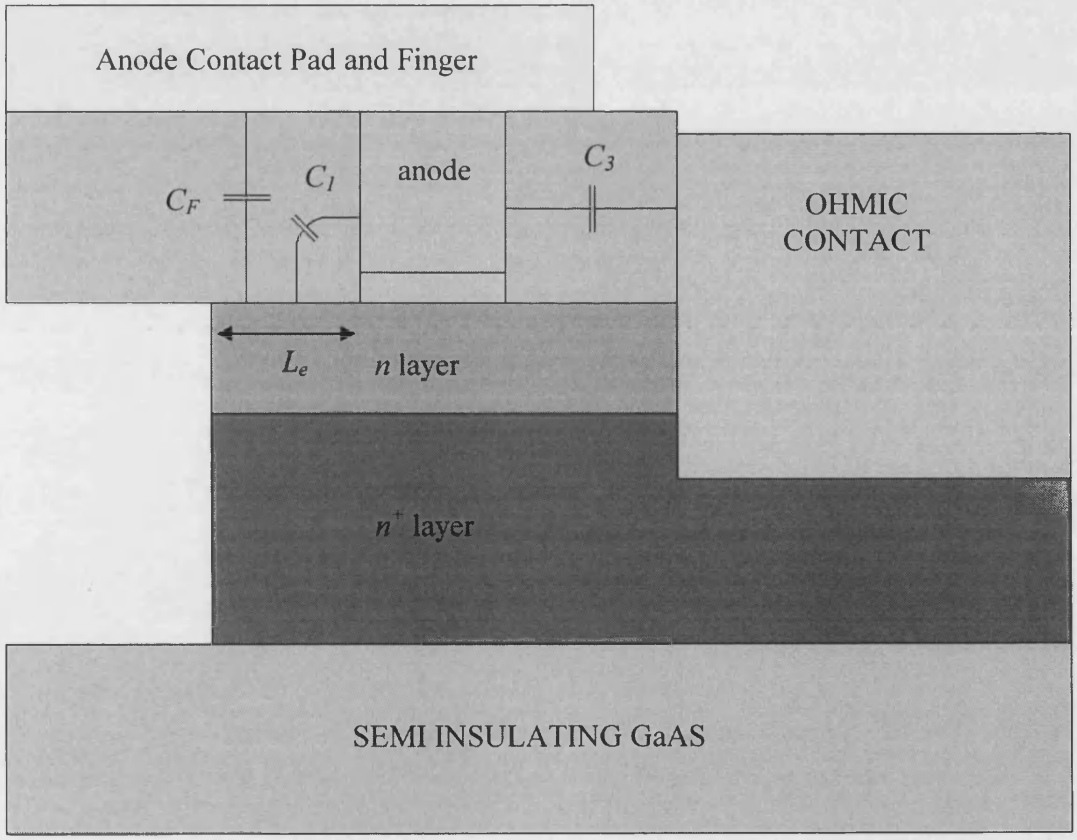


Fig. 4.13 Parasitic capacitances within the planar diode. C_1 is the capacitance due to the anode cone and the material beneath it, C_F the capacitance given between the GaAs and anode contact finger and C_3 is the capacitance between anode and ohmic contact.

C_1 has been evaluated by Kerr [4.28] and is given by

$$C_1 = \frac{\pi\varepsilon\left(a_0^2 - b_0^2\right)^{1/2}}{\tan^{-1}\left[\dfrac{\left(a_0^2 - b_0^2\right)^{1/2}\tan\left(\dfrac{\phi_a}{2}\right)}{\left(a_0 + b_0\right)}\right]} \tag{4.27}$$

where

$$a_0 = r_0 \ln\left(\frac{r_2 - r_0}{r_1 - r_0}\right)$$
$$b_0 = r_2 - r_1 \tag{4.28}$$

and all radii are shown in Fig. 4.14.

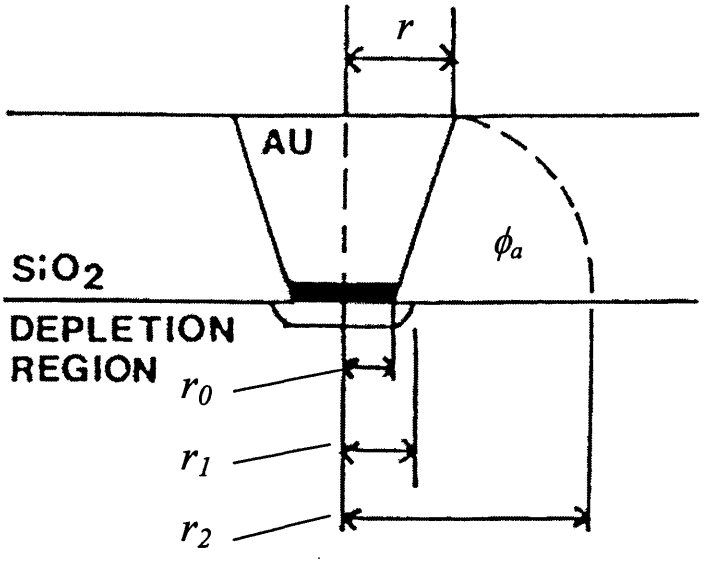


Fig. 4.14 The radii and angle needed for calculating C_1, [4.25]

C_F is the capacitance between the *n* GaAs and contact finger and is given by [4.25]

$$C_F = 2.5\varepsilon L_e \tag{4.29}$$

where L_e is the portion of the finger that overhangs the active GaAs as shown in Fig. 4.13. The capacitance between the anode and the ohmic contact, C_3, is given by [4.29]

$$C_3 = \frac{2\pi\varepsilon t_{ox}}{\ln(r_x/r)} \tag{4.30}$$

where t_{ox} is the thickness of the oxide layer. The total shunt capacitance is the sum of C_1, C_F and C_3.

4.4 Diode Optimising

Optimising the diode for maximum multiplier performance was carried out during the Harmonic Balance analysis discussed in Chapter 6. This involved optimising the anode diameter, length and width of contact finger and the optimum diode bias and input power. However, initial modelling was undertaken using the following approach.

Lin et al. [4.30] base their diode optimising on the principle that the maximum change rate of the depletion layer cannot exceed the saturation velocity in the *n* layer. They use this principle to optimise the doping concentration of the *n* layer and the results are shown in Fig. 4.15.

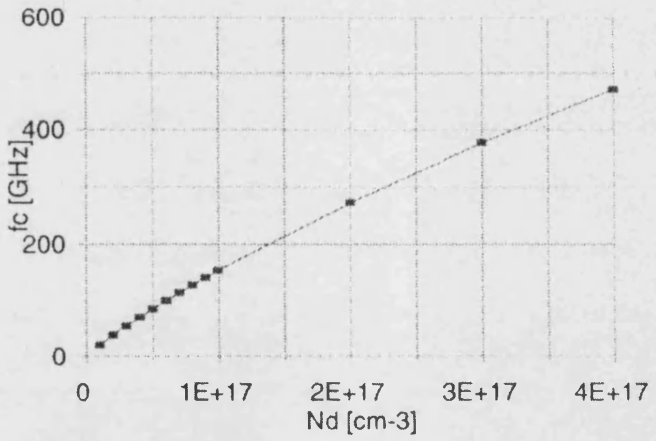


Fig. 4.15 Maximum pump frequency as a function of doping concentration, [4.30].

Louhi et al. [4.31] offer a method for optimising the thickness of the epilayer. The change in depletion layer width during the pump cycle of the diode given by

$$\Delta w = \frac{v_{e,\max}}{2f_{out}} \tag{4.31}$$

where f_{out} is the output frequency. An optimum value of t_e can be found, according to Louhi, by adding a few hundredths of a micron to the maximum modulation of the depletion layer width.

In the case of a multiplier with an output frequency of 200 GHz and a GaAs epilayer the change in depletion layer width over a pump cycle should be around half a micron. However when reverse biasing the diode the depletion layer can be extended by up to approximately half a micron as shown in Table.1 using equation (4.3).

V_b (V)	w (μm)
0	0.08
-2	0.19
-4	0.25
-6	0.30
-8	0.35
-10	0.39
-12	0.42

Table.1 Variation of epilayer depletion width with applied reverse bias.

Using equation (4.31) the maximum change of the depletion layer width when operating at 200 GHz will be 0.55 μm. Therefore when the varactor is reversed biased to a value of 8 V and oscillates at 200 GHz, the resulting change in depletion region width can be seen to oscillate around the fixed reverse bias depth. This is illustrated in Fig. 4.16a. At 8 V reverse bias the depletion width is at 0.35 μm and at 200 GHz the maximum change in depletion width is 0.55 μm giving the maximum depletion width to a value of ~ 0.6 μm, as shown in Fig. 4.16b.

It is therefore possible to say that with an output frequency of 200 GHz and a reverse bias of 8 V that the optimum epilayer thickness should be, according to Louhi [4.31], approximately 0.62 μm.

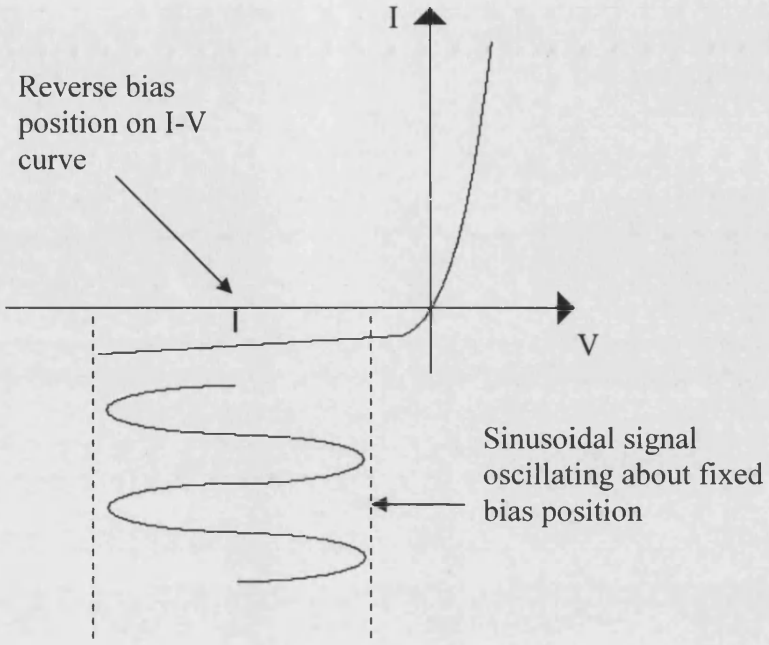


Fig. 4.16a Varactor I-V characteristic showing sinusoidal signal oscillating about the fixed bias position.

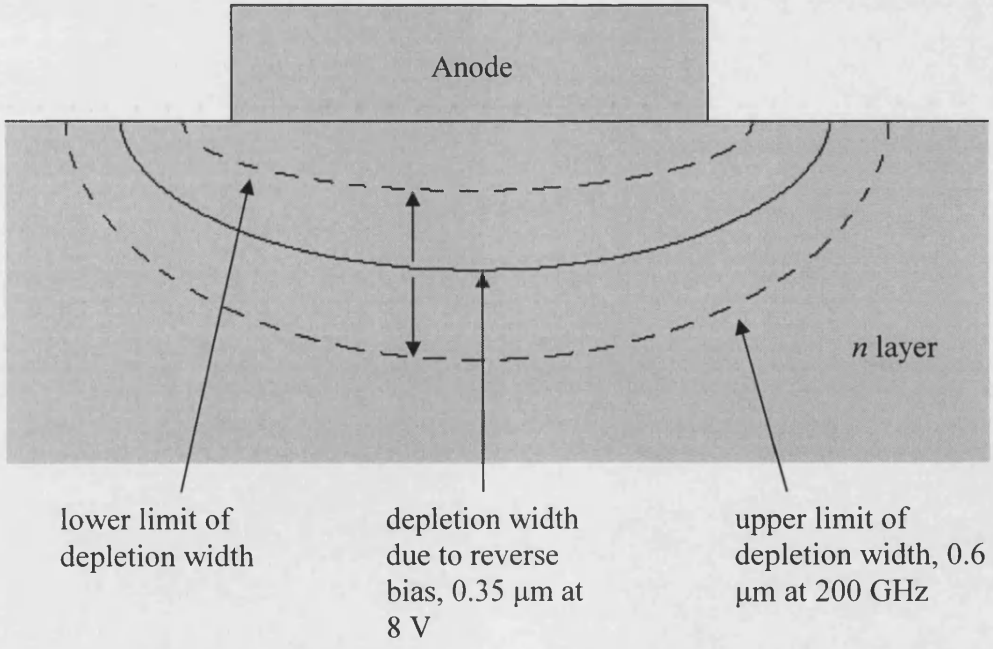


Fig. 4.16b Showing upper and lower limits to the depletion region width resulting from the sinusoidal signal oscillating about the fixed bias position.

References – Chapter 4

[4.1] F. Braun, "On current conduction through metallic sulphides," *Ann. Phy. Chem.*, vol. 153, December 1847, pp. 377-380 (translated)

[4.2] W. Schottky, "Semiconductor theory in the blocking layer," *Naturwissenschaften*, vol. 26, December 1938, p. 381 (translated)

[4.3] N. F. Mott, "Note on the contact between a metal and an insulator or semiconductor," *Proc. Cambridge Philos. Soc.*, vol. 34, October 1938, pp. 568-572.

[4.4] H. A. Bethe, "Theory of the boundary layer of crystal rectifiers," *MIT Radiat. Lab. Rep.*, November 1942, pp. 387-399.

[4.5] A. M. Goodman, "Metal-semiconductor barrier height measurement by the differential capacitance method-one carrier system," *Journal of Applied Physics*, vol. 34, no. 2, February 1962, pp. 400-409.

[4.6] M. T. Faber, J. Chramiec, M. E. Adamski, "Microwave and millimeter diode frequency multipliers," *Artech House, Inc, MA*, 1995.

[4.7] S. M. Sze, "Physics of semiconductor devices," *New York: John Wiley and Sons*, 1969.

[4.8] J. T. Louhi, A. V. Raisanen, "Dynamic shape of the depletion layer of a submillimeter-wave Schottky varactor," *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 12, December 1996, pp. 2159-2164.

[4.9] J. T. Louhi, A. V. Raisanen, "On the modelling and optimization of Schottky varactor frequency multipliers at submillimeter wavelengths," *IEEE Trans. On Microwave Theory and Techniques*, vol. 43, no. 4, April 1995, pp. 922-926.

[4.10] J. T. Louhi, "The capacitance of a small circular Schottky diode for submillimeter wavelengths," *IEEE Microwave and Guided Wave Lett.*, vol. 4, 1994, pp. 107-108.

[4.11] B. Gelmont, *et al.*, "Capacitance-voltage characteristics of microwave Schottky diodes," *IEEE Trans. on Microwave Theory and Tech.*, vol. 39, no. 5, May 1991, pp. 857-862.

[4.12] V. Shashkin, *et al.*, "Planar Schottky diodes with low barrier height for microwave detector application," *Proc. 23rd International Conference on Microelectronics*, vol. 1, May 2002, pp. 335-338.

[4.13] C. R. Crowell, S. M. Sze, "Current transport in metal-semiconductor barriers," *Solid-State Electronics*, vol. 9, 1966, pp. 1035-1048.

[4.14] C. R. Crowell, "Richardson constant and tunneling effective mass for the thermionic and thermionic-field emission in Schottky barrier diodes," *Solid-State Electronics*, vol. 12, 1969, pp. 55-59.

[4.15] C. Y. Chang, S. M. Sze, "Carrier transport across metal-semiconductor barriers," *Solid-State Electronics*, vol. 13, 1970, pp. 727-740.

[4.16] F. A. Padovani, R. Stratton, "Field and thermionic-field emission in Schottky barriers," *Solid-State Electronics*, vol. 9, 1966, pp. 428-440.

[4.17] S. J. Pilkington, *et al.*, "On the Richarson constant of intimate metal-GaAs (111)B Schottky diodes grown by molecular beam epitaxy," *J. Appl. Phys.*, vol. 74, no. 10, November 1993, pp. 6256-6260.

[4.18] P. A. Verlangieri, *et al.*, "Low-resistance ohmic contacts for microwave and lightwave devices," *IEEE Microwave and Guided Wave Letters*, vol. 1, no. 3, March 1991, pp. 51-53.

[4.19] R. Williams, "Modern GaAs processing methods," *Artech house*, 1990.

[4.20] E. L. Kollberg, *et al.*, "Current saturation in submillimeter wave varactors," *IEEE Trans. on Microwave Theory and Tech.*, vol. 40, no. 5, May 1992, pp. 831-838.

[4.21] N. Erickson, "High efficiency submillimeter frequency multipliers," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. III, 1990, pp. 1301-1304.

[4.22] L.E. Dickens, "Spreading resistance as a function of frequency," *IEEE Trans. On Microwave Theory and Techniques*, vol. MTT-15, no. 2, February 1967.

[4.23] K. McKinney, *et al.*, "Design, fabrication, and performance of a whiskerless Schottky diode for millimetre and submillimeter wave applications," *IEEE Proc. Southeastcon*, April 1985, pp. 111-115.

[4.24] D. G. Garfield, *et al.*, "Design, fabrication, and testing of a novel planar Schottky barrier diode for millimetre and submillimeter wavelengths," *IEEE Proc. Southeastcon*, April 1988, pp. 154-160.

[4.25] C. H. Blanton, M.S. Thesis, University of Virginia, 1984.

[4.26] C. S. Setzer, Dissertation, University of Virginia , 1981.

[4.27] W. L. Bishop, "A novel whiskerless Schottky diode for millimetre and submillimeter wave applications," *IEEE MTT-S Digest*, vol. Q-16, 1987, pp. 607-610.

[4.28] A. R. Kerr, *et al.*, *NASA Technical Memo.*, no. 79616, 1978.

[4.29] W. H. Hayt, "Engineering Electromagnetics," McGraw-Hill, New York, 1981.

[4.30] C-I. Lin, *et al.*, "Planar Schottky diodes for submillimeter wave applications," *Terahertz Electronics Proceedings*, IEEE Sixth International Conference, 3-4 September 1998, pp. 135-138.

[4.31] J. T. Louhi, A. V. Raisanen, "Optimization of the Schottky varactor for frequency multiplier applications at submillimeter wavelength," *IEEE Microwave and Guided Wave Letters*, vol. 6, no. 6, June 1996. pp. 241-242.

Chapter 5

Structure Simulation

It is critical to understand how the multiplier structure behaves under RF conditions. Conventionally this is done with scale modelling where a replica of the multiplier is made on a much larger scale which is easier to measure and manipulate. With the onset of finite element analysis (FEA) packages, such as Ansoft's HFSS, and more powerful desktop computers it is possible to model these structures at almost any frequency. This gives the designer a certain element of freedom to the structures that can be tested using a simple CAD environment. By using wave ports in the computer structure or coaxial feed lines in a scale model the embedding impedance can be determined for the multiplier structure. The embedding impedance is the key element used in the harmonic balance analysis (see Chapter 6) to determine the multiplier performance.

This chapter discusses the scale and computer modelling of the multiplier structure and the steps taken to ensure this was as accurate as possible. Any computer generated results are backed with practical ones wherever possible.

5.1 Multiplier Design

The basic design of the multiplier structure is shown in Fig. 5.1. The multiplier has a crossed waveguide layout connected by a small suspended microstrip cavity. The input guide (WR10) is comprised of three sections. The first section at full height is where the input signal will arrive from the source. The second section is an impedance transformer where the full height guide is reduced down to just under ¼ of the standard dimension, (2.54 x 1.27 mm to 2.54 x 0.30 mm). The third section is reduced height and is over two guided wavelengths in length.

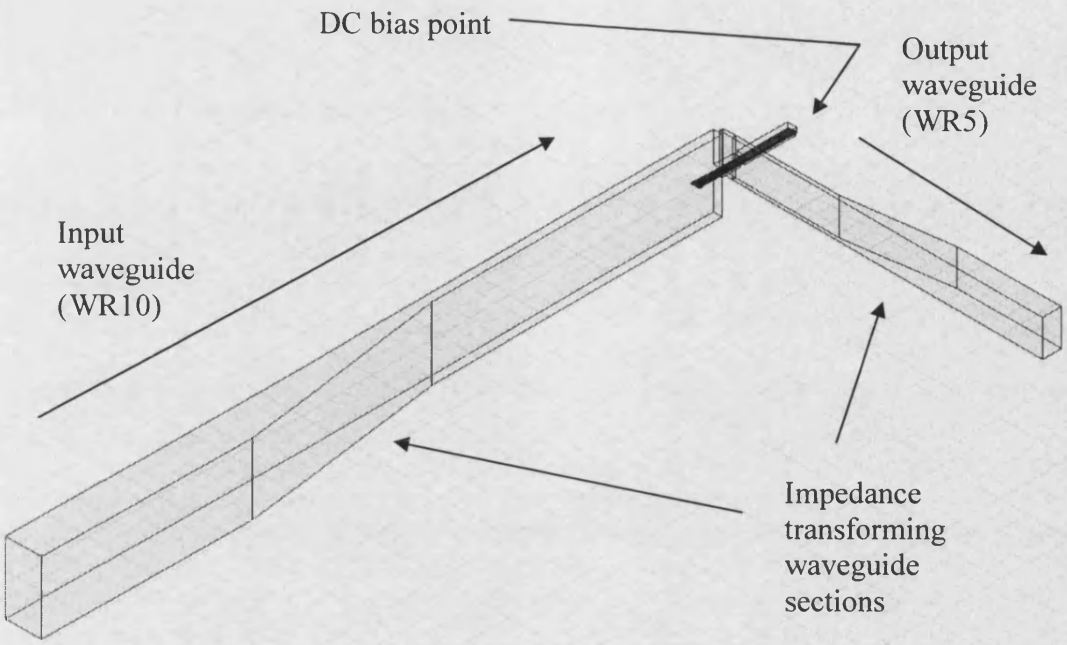


Fig. 5.1 3D representation of multiplier showing input and output waveguides

There are four reasons why the input guide is reduced in height:

1. Reduce waveguide impedance
2. Suppress parasitic modes
3. Reduce labour in fabricating multiplier block
4. Maximize chip yield from single mask

The reduction in waveguide impedance enables better matching of the devices (the diodes) to the rest of the circuit. Suppression of parasitic modes at the output frequency was needed in the input guide because of the multiplier design. Since the diodes were located in the input guide it was possible that coupling would occur at the output frequency and output power lost down the input guide. Suppressing these modes ensured all available power was transmitted to the output circuit (see section 5.3.3 for an example of mode suppression). Reducing the guide height also made constructing the block easier as a single milling tool could cut the guide and cavity with a simple step in height which improved accuracy of the block dimensions. Finally, the GaAs chip width had a direct impact on the number of devices that can

fit on a single 10 x 10 mm cell of a photolithographic mask. If a wider input guide was used the chip would have to be wider to provide contact to the waveguide walls or a bond wire would have to be used, increasing fabrication difficulty.

The output guide was designed with the same three sections: reduced height, transforming and full height (WR5). The transforming section takes the full height WR5 guide to $^{3}/_{8}$ original height (1.295 x 0.648 mm to 1.295 x 0.243). Fig. 5.2 is a closer view of a section of Fig. 5.1 and shows the multiplier chip located in the suspended microstrip cavity. Fig. 5.2 also shows detail of the microstrip transmission line, the microstrip filter and the output backshort. The backshort, as described in Chapter 2, can be moved during the modelling to find optimum position to give the best impedance match between the output waveguide and the quasi-microstrip section that spans it. This small section of semiconductor and metal act as an antenna to the output guide, radiating power at the output frequency down the waveguide to the output. The microstrip filter in Fig. 5.2 provides an effective short circuit to fundamental and higher order harmonics whilst maintaining an unbroken electrical path to the diodes for biasing. The gallium arsenide substrate was thinned down to a membrane to reduce dielectric loading of the system and reducing overall RF losses. The membrane was mechanically sturdy enough to support its own weight as it formed a type of rigid cantilever out of the cavity.

Fig. 5.3 shows a closer view of the end of the membrane where the location of the varactor diodes are indicated on the diagram, either side of a central transmission line which extends towards the output waveguide. Each diode has an adjacent tab that is used to solder a connection to the waveguide wall. This connection provides the DC voltage path required to apply a reverse bias to each diode. The connection is also required to allow currents at the fundamental RF frequency to couple into the diodes efficiently.

Fig. 5.3 also shows the presence of the diode air-bridge which connects the diodes anode to the central transmission line. The air-bridge isolates the diodes from each other on a single multiplier chip and provides a reduction in parasitic capacitance by removing the highly doped material from below the anode finger (see Chapter 4).

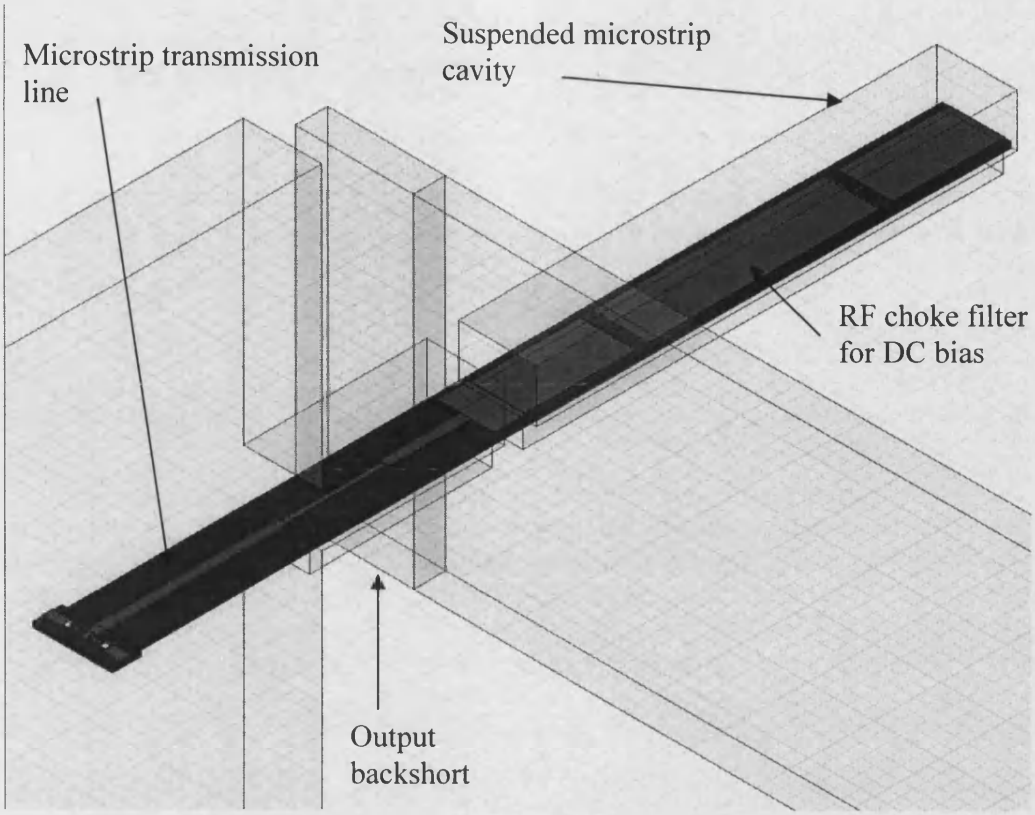


Fig. 5.2 Closer view of Fig. 5.1 showing suspended GaAs membrane substrate and RF filter.

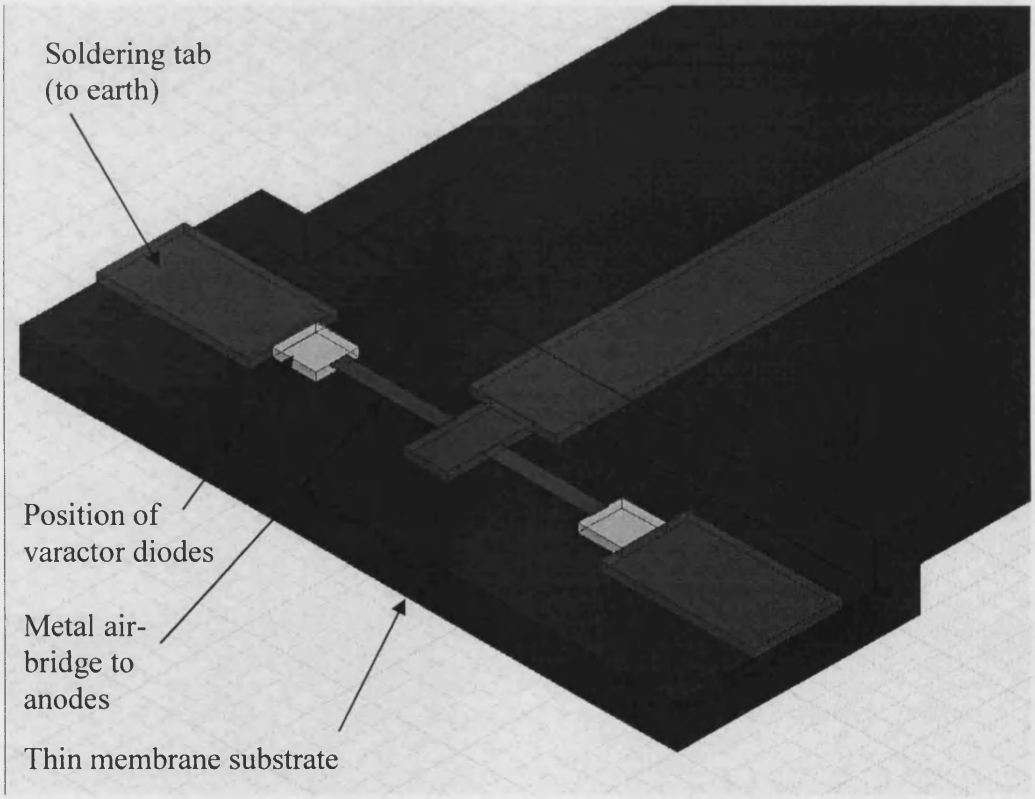


Fig. 5.3 Multiplier structure showing varactor positioning, location of the diode air bridges and the soldering tabs at either side of the chip to provide an earth to the waveguide walls.

The symmetric design inside the input waveguide puts the diodes in a balanced anti-series configuration (see Chapter 2). This configuration suppresses odd harmonics to a virtual loop inside the diodes and are of no further consequence to the multiplier circuit. This configuration is highly desirable from the point of reducing circuit design and fabrication labour with one drawback, the input waveguide can have no moving backshort. This limits the multiplier bandwidth somewhat and so the distance between the diodes and the terminating wall in the input waveguide was the most critical dimension to be decided by the structure modelling. This dimension of length is termed here the *effective backshort length* and abbreviated to L_{eff}.

5.2 Input Circuit Optimising

With any simulation or modelling it is always important to confirm results with two or more different methods before they can be considered a sound prediction. As the outcome of this chapter is heavily weighted on computer modelling it was important to ensure the computer simulations were reliable and, hence, needed to be verified with scale modelling

The input circuit can be defined anywhere where currents will flow at the fundamental frequency. For the multiplier in this work the input circuit is relatively simple. Attention was needed when designing the circuit to efficiently couple the input signal from the waveguide to the microstrip transmission line. Waveguide-to-microstrip transmission is of much importance to RF engineers and is well documented, [5.1, 5.2]. Conventionally coaxial lines are used to couple signals from the waveguide to the diodes, [5.3]. To improve integration of the diodes to the rest of the circuit microstrip probes have been an invaluable step forward.

Conventionally the waveguide and the cavity holding the microstrip are perpendicular to each other with the microstrip entering the waveguide through the broad wall of the guide as shown in Fig. 5.4.

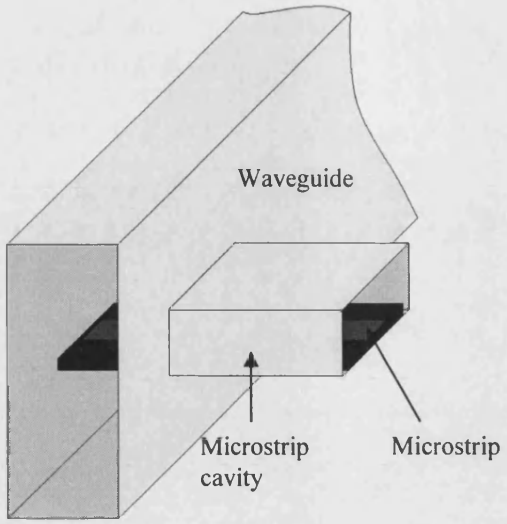


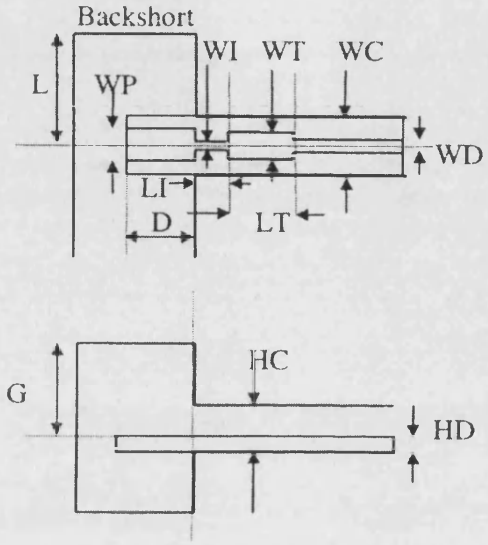
Fig. 5.4 Conventional waveguide to microstrip transmission where the microstrip cavity penetrates the broad wall of the waveguide centrally and the substrate is carried into the waveguide. The metal microstrip track is indicated on the diagram running down the centre of the substrate.

5.2.1 Computer Modelling

When designing the microstrip to waveguide transmission network the parameters will greatly depend on the individual case; width of the substrate, substrate material used, size of the cavity and any non-passive components involved. However, Leong and Weinreb performed a study using HFSS to give a full band conversion for any waveguide size (with a 2:1 aspect ratio) to a microstrip with several different substrate materials [5.2]. The details of the parameters used are shown in Fig. 5.5(a) and the values for a WR10 waveguide in Fig. 5.5(b) for 5 different substrate materials. The values in Fig. 5.5(b) can be scaled to any waveguide size by multiplying the dimension listed in the table by a scaling factor equal to (width of target waveguide in um)/2540.

Leong and Wienreb observed a relationship between probe width, WP, probe length, D, and backshort distance, L, in all the experiments they performed. They looked for the variation in impedance seen at the broad (waveguide) wall window with respect to the above parameters. They found the impedance at the window to have 50 Ω or less real impedance and have a capacitive reactance necessitating the need for impedance transformers. The first impedance transformer, WI & LI, is a high impedance inductive line to series resonate out the capacitive reactance. The second, WT & LT, is a quarter wave impedance transformer to match the real part of the

probes impedance back to 50 Ω. The generic form of this information was useful up to a point, the parameters would obviously need to be altered if they were, for example, not transmitting down a 50 Ω microstrip line. However the analysis gave good coupling efficiency when tested in HFSS and the results are shown in Fig. 5.6 (b) along with an image of the model used in Fig. 5.6 (a). Fig. 5.6 (b) shows less than 0.8 dB loss between 80 and 115 GHz for the waveguide to microstrip transition.

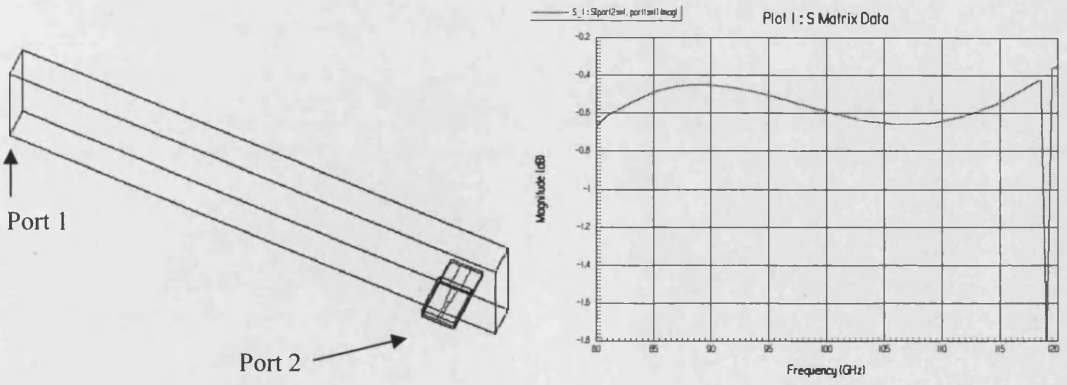


(a)

#	Probe	Er	L	HC	HD	WC	WP	D	WI	LI	WT	LT	G	WD
1	Teflon-127	2.2	838	259	127	973	324	635	80	100	-	-	1270	230
2	Teflon-76	2.1	838	254	76	508	230	660	120	260	-	-	1270	210
3	Diel6-127	6.0	876	259	127	740	291	600	80	100	180	420	1270	140
4	Alumina-100	10.1	876	259	100	508	200	600	50	100	130	350	1270	80
5	GaAs-100	13.0	908	259	100	740	259	560	40	60	130	320	1270	70

(b)

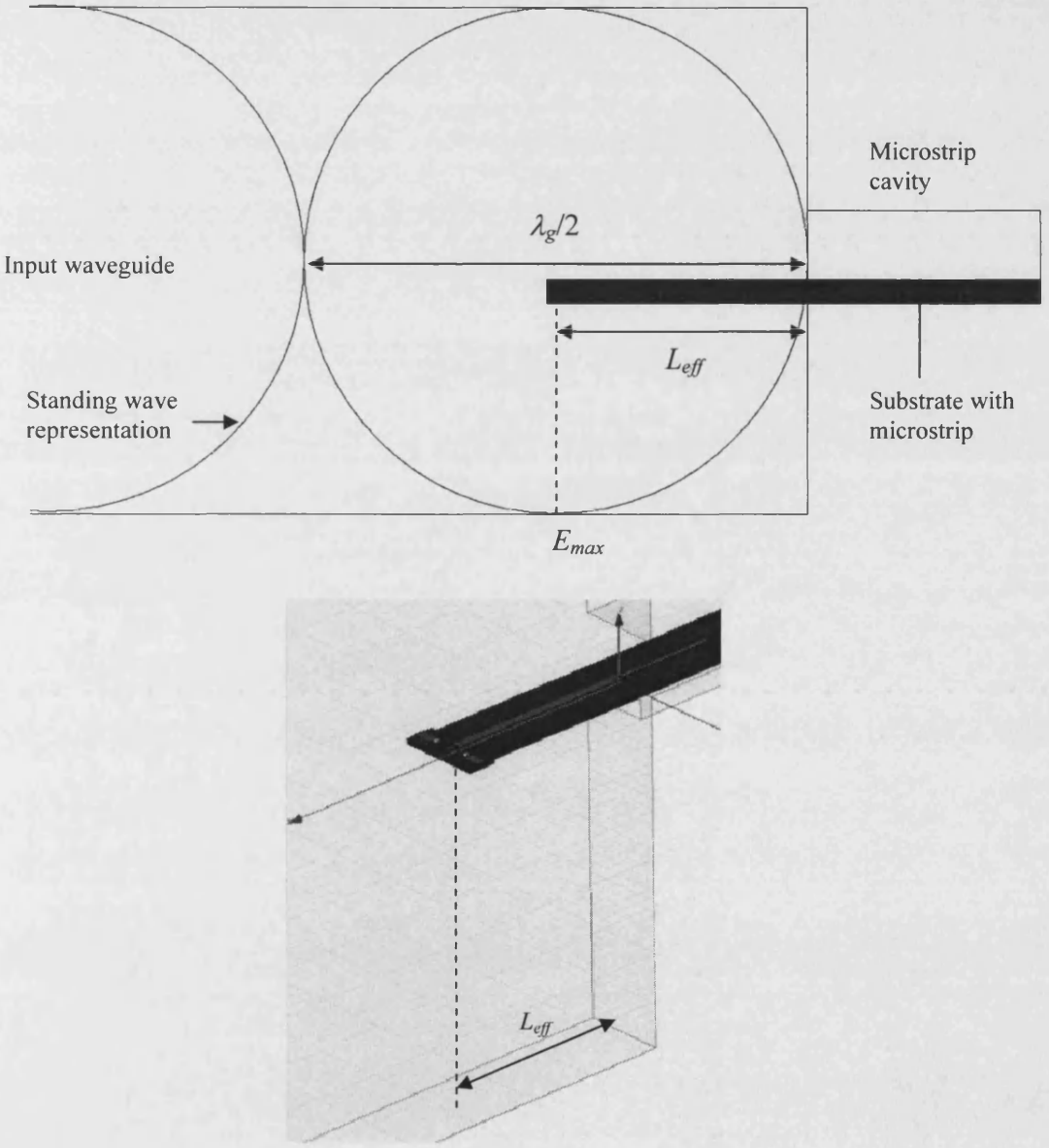
Fig. 5.5 Showing (a) parameters for microstrip to waveguide transmission and (b) parameter values for different substrate materials, [5.2].



(a) (b)

Fig. 5.6 Showing (a) the model used in HFSS and (b) the S_{21} response where port 1 is defined as the waveguide port and port 2 is defined as the window in the cavity.

The design in Fig. 5.6(a), however, was considerably different to the design of the multiplier and several modifications were needed. First the backshort length L became the effective backshort length L_{eff} and the cavity now appeared through the end wall not the broad wall. The waveguide height had to be taken down from full height to 0.3 mm and the substrate needed to be narrower and thinner. This, naturally, changed the impedance of the probe and waveguide and the model had to be optimized for the new parameters.



(b)

Fig. 5.7 Representation of (a) a standing wave scenario in the input waveguide of the multiplier showing a superposition of the standing wave, the microstrip cavity and substrate. λ_g is the guided wavelength at the fundamental frequency in the input guide, (b) a 3D view showing L_{eff}.

Fig. 5.7(a) represents the multiplier input waveguide and microstrip cavity indicating the position of the substrate and a superimposed standing wave at the fundamental frequency. The terminating wall acts as the short circuit for the waveguide transmission line and the microstrip cavity is small enough that no TE waveguide modes are supported. In this case the maximum electric field, E_{max}, should occur at $\lambda_g/4$ from the backshort but due to the presence of the substrate and cavity this was not always the case. This was, theoretically, where maximum coupling efficiency from waveguide to microstrip should occur. Fig. 5.7 (b) illustrates the variable L_{eff}.

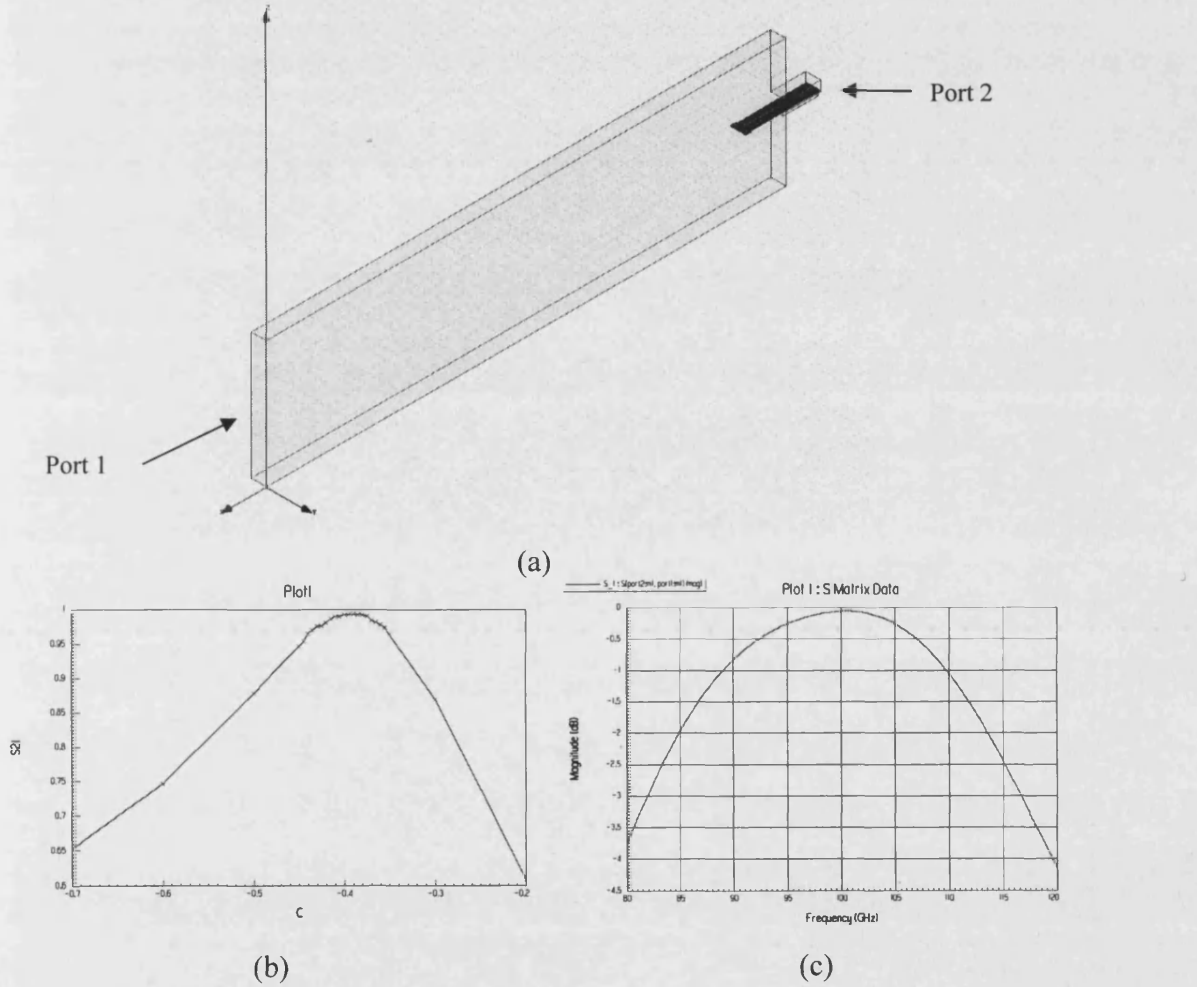


Fig. 5.8 Showing (a) HFSS model of the two port network used to determine optimum L_{eff} for the passive structure, and graphs showing (b) S_{21} network response as a function of C where $L_{eff} = |C|+0.4$ and (c) the frequency response of the two port network at the optimum effective backshort position.

The model in Fig. 5.8(a) was used to determine the optimum value of L_{eff} for a passive structure containing no diodes. Using a simple two port network (port 1

being the input waveguide window and port 2 being the output window of the cavity) the highest coupling efficiency between the two ports (S_{21} closest to zero) was found by varying L_{eff}. Fig. 5.8(b) & (c) show two graphs produced in HFSS for the two port network. Fig. 5.8(b) shows the S_{21} response when the parameter C was swept between -0.2 and -0.7 where $L_{eff} = |C|+0.4$. This indicated a peak in the coupling efficiency at $L_{eff} = 0.79$ mm. Fig 5.8(c) indicates the frequency response of the two port network at the optimum value of L_{eff}. The 3dB bandwidth of this network is ~35% of the centre frequency which is not as broadband as the microstrip to waveguide probe described by Leong & Weinreb but adequate given the restrictions imposed by our design, e.g. waveguide height and substrate thickness.

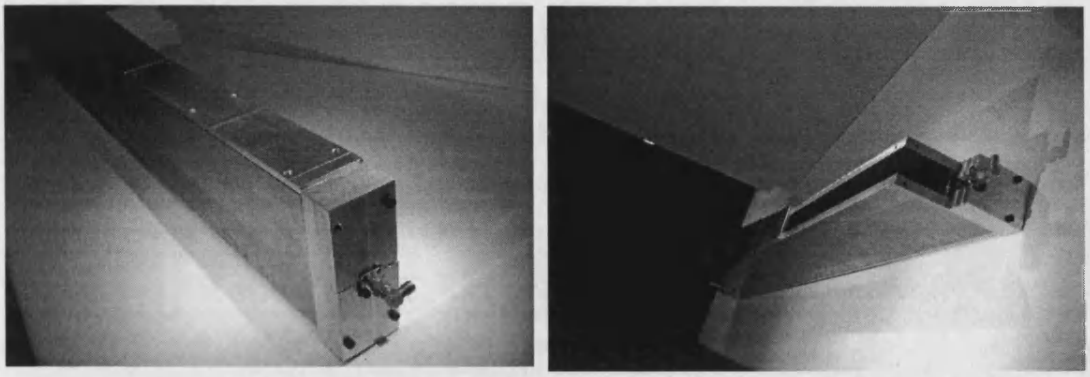
5.2.2 Scale Modelling

The scale model is a practical solution for determining RF network properties. According to Stratton [5.4] the electromagnetic parameters remain identical through scaling when k_1 and k_2 are constant. The scaling identity is given by

$$k_1 = \mu\varepsilon(\omega d)^2 \tag{5.1}$$

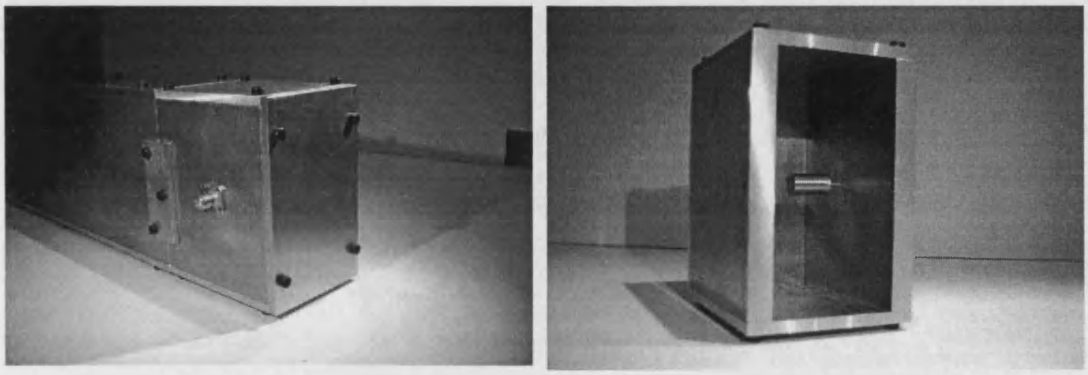
$$k_2 = \mu\sigma\omega d^2 \tag{5.2}$$

where μ is the permeability, ε is the permitivity, ω is the angular frequency, d is a dimension and σ is the conductivity. If the frequency of a model is reduced the dimensions of the model will change and according to (5.1) changes may have to be made to the permittivity in order for k_1 to remain constant. A fundamental operating frequency of 3 GHz was chosen for the scale model as a trade-off between scale model size and network analysis equipment frequency limitations. Using (5.1) and (5.2) the scaling factor was found to be 33 $^1/_3$ in order to keep k_1 and k_2 constant. Photos of the aluminium scale model are shown in Fig. 5.9. Fig. 5.9(a) and (b) show the reduced height end of the input waveguide where an SMA connector acts as port 2. Fig 5.9(c) and (d) show the opposite end of the waveguide, at full height, where an SMA connector (external) is attached to a waveguide launcher (internal) which allows a signal to be transmitted into the waveguide with a known high efficiency and good bandwidth. This section acted as port 1. Fig. 5.9(e) and (f) show a closer view of the microstrip cavity and waveguide microstrip probe.



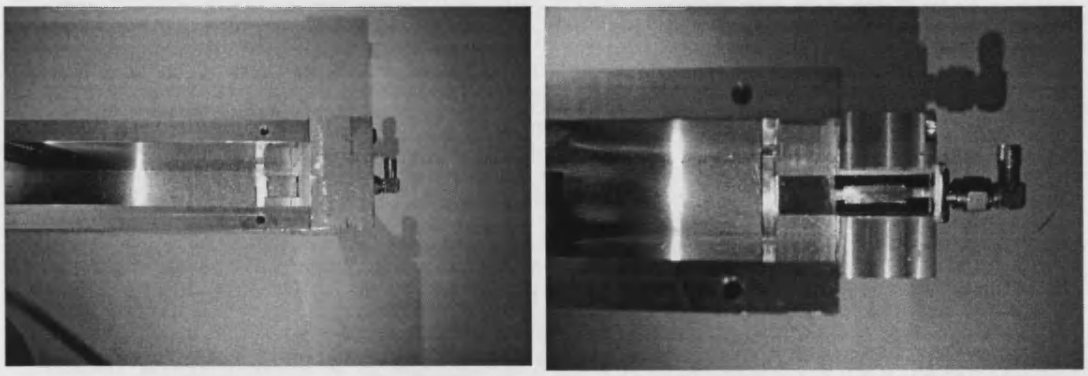
(a) (b)

Fig. 5.9 Showing (a) SMA connector to microstrip cavity at reduced height waveguide end and (b) with top plate removed and cavity block split down symmetric plane.



(c) (d)

Fig. 5.9 Showing (c) SMA connector to the waveguide launcher of the input waveguide at full height and (d) the waveguide launcher probe inside the full height input waveguide.



(e) (f)

Fig. 5.9 Showing (e) a closer view of the microstrip probe in the reduced height input waveguide and (f) again with the top half of the split block cavity section removed showing the impedance transformer and the coaxial SMA connector contacted to the copper microstrip using a silver conducting paint.

The substrate was fabricated from semi-insulating gallium arsenide and the microstrip was cut out of some adhesive copper tape. A series inductor and quarter wave transformer were made in the microstrip similar to that show in Fig. 5.5(a).

The results of the scale model S_{21} response are shown in Fig. 5.10. The frequencies for the scale model have been scaled up to correspond to that of the HFSS model.

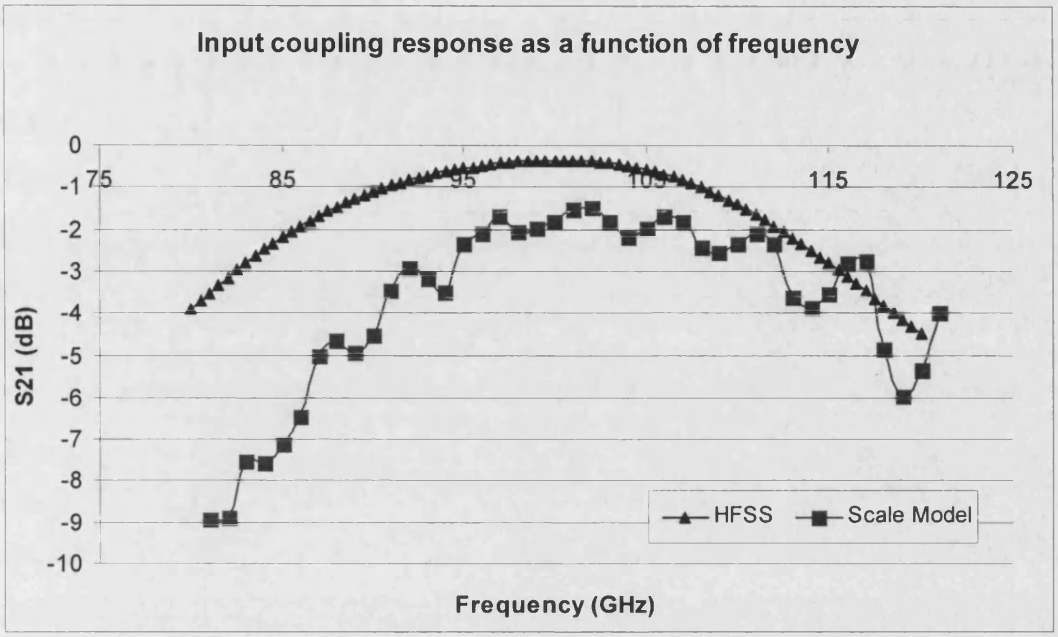


Fig. 5.10 S_{21} waveguide to microstrip response comparison between the scale model and the HFSS model.

The difference between the two sets of data in Fig. 5.10 arise from a number of irregularities between the two models. The differences between the two models can be put down to the following observations.

- Inaccuracies in cutting the copper foil microstrip to the exact size.
- Scale model waveguide launcher had good but not lossless transmission into the guide resulting in lower S_{21} for the scale model.
- Placing the scale model copper microstrip probe in the input guide at the slightly wrong position resulted in a shift in the S_{21} peak.
- HFSS draws the *perfect* model, no imperfections or irregularities in the waveguides or cavities, dimensions are more precise than can be mechanically made.

5.3 Output Circuit Optimising

The output circuit should allow the current at the second harmonic to be transmitted from the diodes to the output waveguide with minimal loss and with the highest

possible bandwidth. The output backshort has to be set to the optimum position so the output frequency is centred at 200 GHz. Also of great importance is the RF choke filter that provided an effective short circuit at all possible RF frequencies. If this filter is not adequate output power will be lost down the cavity.

5.3.1 Output Backshort

The output backshort for the multiplier was fixed and so it was critical to get the modelling correct as the backshort could not be adjusted once it was fabricated. The output backshort provided impedance tuning between the suspended quasi-microstrip section and the output waveguide

The backshort position was optimized by using an HFSS model consisting of the microstrip cavity and the output waveguide as shown in Fig 5.11. A 200 GHz signal was injected into the model via port 1 and the transmission coefficients measured at ports 2 and 3. Ideally there should be zero power arriving at port 3 and maximum power transmitted to port 2 at 200 GHz. The HFSS model was used simulate a moving backshort and record the S_{21} in incremental steps. The results could then be plotted and the optimum value of output backshort found at 200 GHz which is shown in Fig. 5.12.

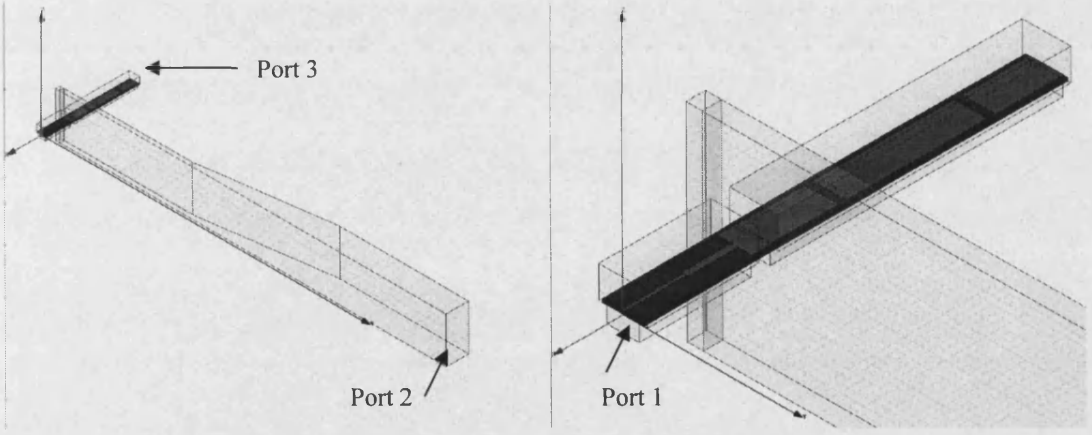


Fig. 5.11 Sowing (a) the HFSS model used to optimize output backshort indicating ports 2 and 3 and (b) indicating port 1.

As with the input circuit, a scale model was constructed of the output circuit to replicate the model in Fig. 5.11. Photos of the scale model are shown in Fig. 5.13. The waveguide and microstrip cavity were constructed out of aluminium. The substrate was made from RT Duroid, a commercially bought material with a relatively high dielectric constant (ε_r = 10.5). The microstrip tracks were lithographically formed using a microstrip design mask, photoresist and a copper etchant.

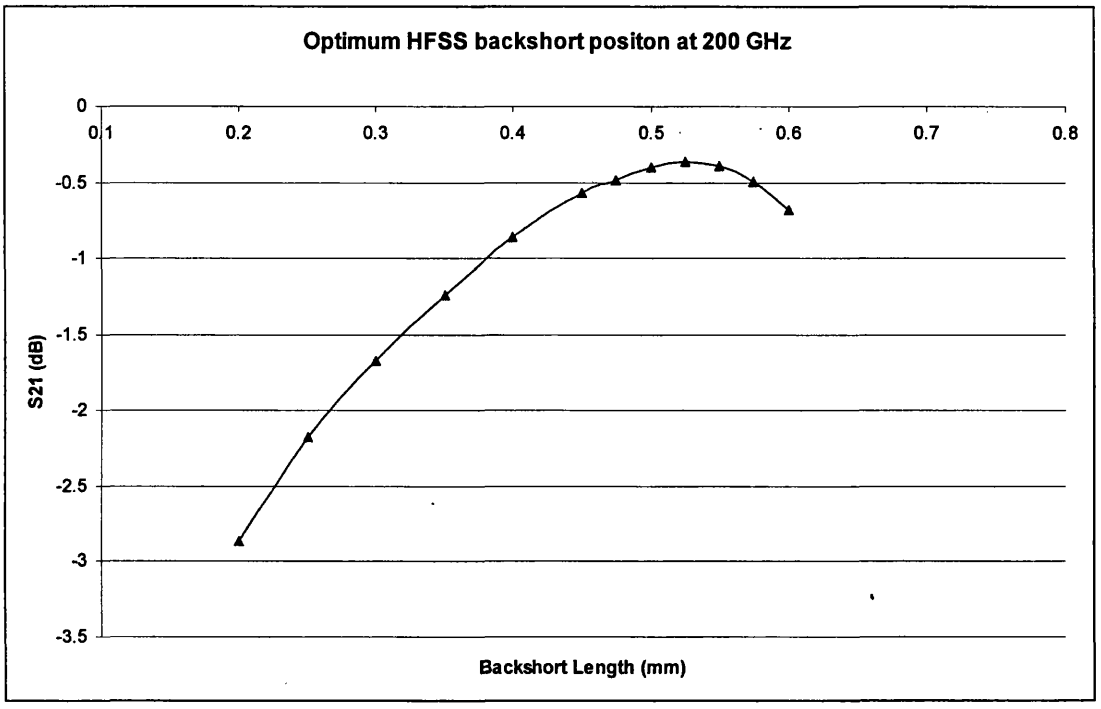
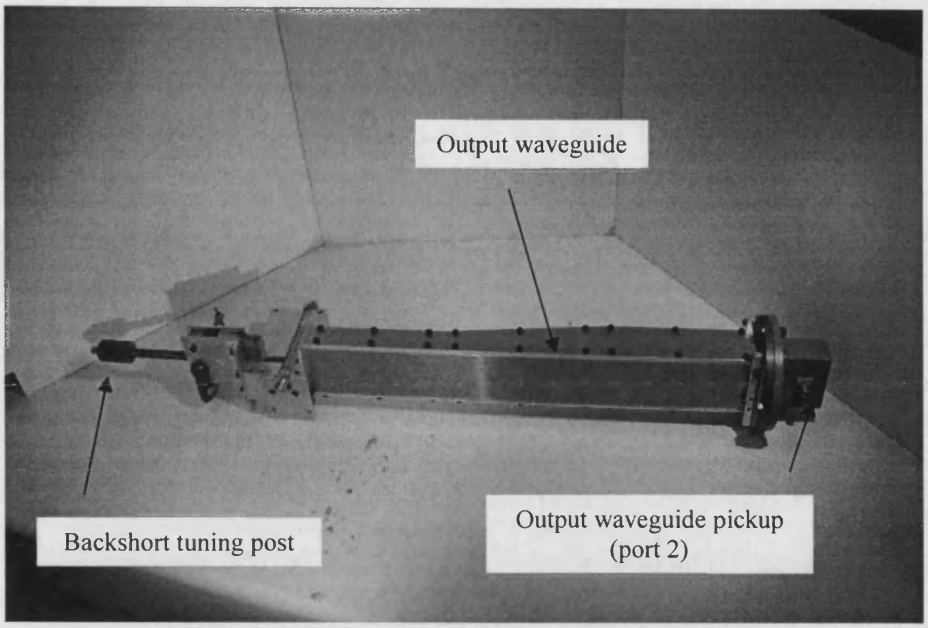
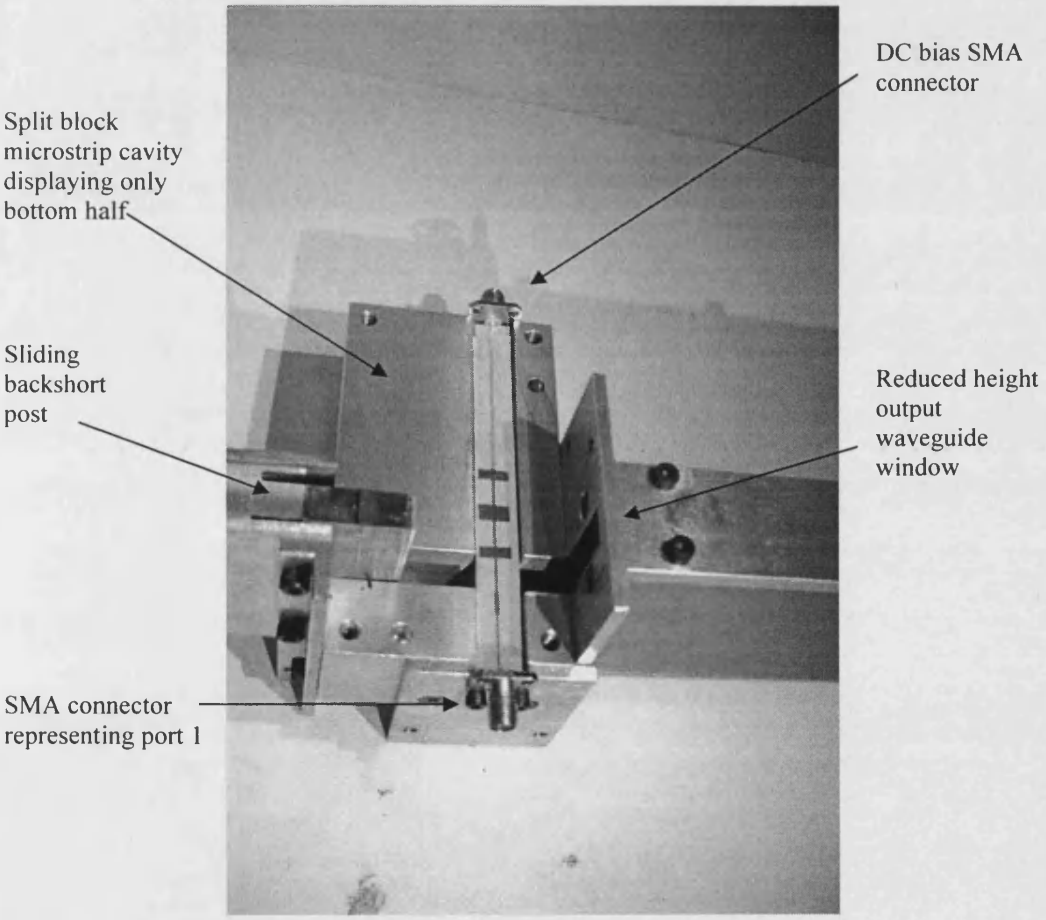


Fig. 5.12 HFSS S_{21} response of the model shown in Fig. 5.9 as a function of backshort position showing an optimum position at 0.525 mm.

A comparison between the HFSS and scale model output circuit response curves are shown in Fig. 5.14. The difference between the plots arises, again, from fabrication tolerances in the scale model and an imperfect backshort. The filter used in the scale model was a first generation type, based on non-suspended microstrip cavity technology, (hence the difference between the HFSS model picture and scale model photograph).



(a)



(b)

Fig. 5.13 Scale model photos of the output circuit showing (a) entire model with backshort tuning post, split block cavity (with top removed) and output waveguide with waveguide pickup and (b) closer view of microstrip cavity showing the SMA connector (port 1), the copper microstrip track and RF filter and sliding backshort post.

The attentive reader may also notice a large difference in S_{21} magnitude between the HFSS plot in Fig 5.12 and of that in Fig. 5.14. The HFSS model in Fig. 5.11 was optimised for a GaAs substrate. Fabricating a scale model substrate in GaAs was difficult and could not be done with precision. This meant using a different substrate (RT Duroid) and filter patterns different to that of the original model. The original HFSS model was then adjusted accordingly to match the scale model with the RT Duroid substrate but was not optimised. Since only a match between the two modelling methods was required (to prove HFSS viability), optimizing the scale model was not deemed necessary hence the difference in S_{21} magnitudes.

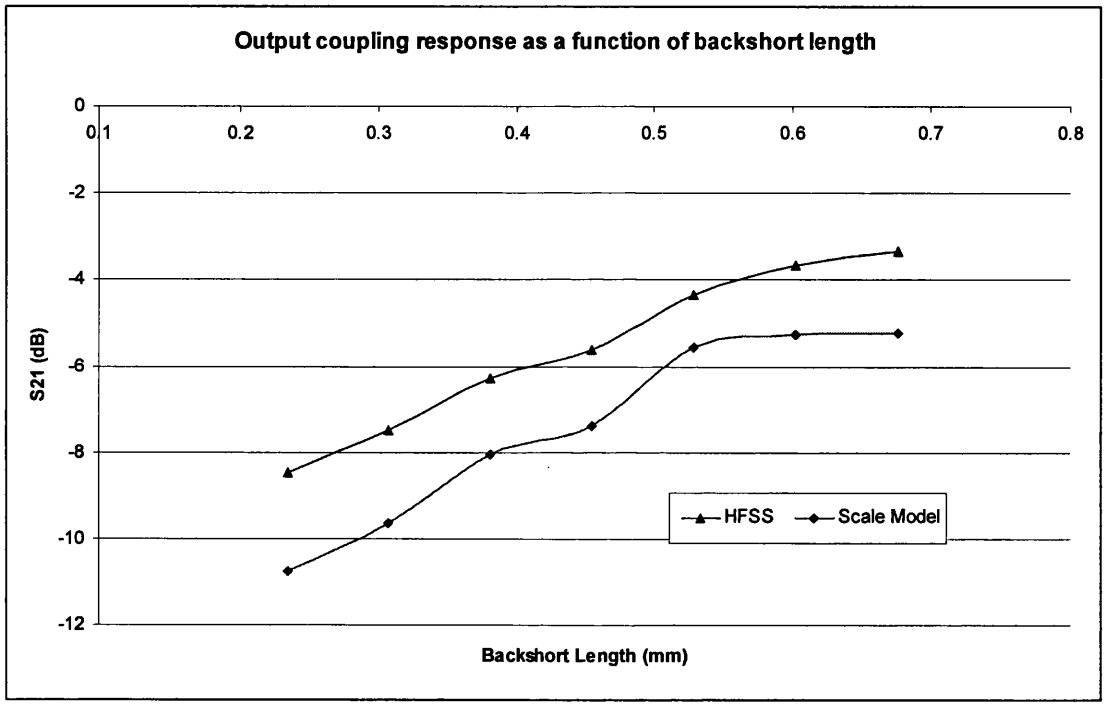


Fig. 5.14 Comparing the S_{21} output circuit responses of the HFSS and scale model as a function of backshort position. The backshort length scale is normalised to the 100 GHz model.

5.3.2 RF Filter

The RF choke filter was preliminarily designed using the Excel spreadsheet referred to in Chapter 2, then modelled in APLAC and then further modelled in HFSS to account for the suspended microstrip cavity. The HFSS model of the filter is shown in Fig. 5.15, split down the symmetric plane where a symmetry boundary is allocated. This was done to reduce convergence time of the program. Since odd harmonics are suppressed in the balanced diode configuration, 190 - 210 GHz was

the main rejection band required from the filter. The frequency response for the filter is shown in Fig. 5.16 giving over 30 dB insertion loss across the entire band.

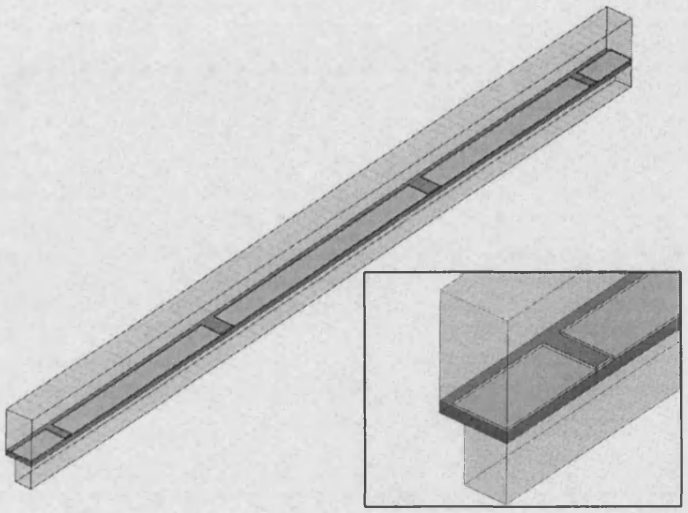


Fig. 5.15 Showing the HFSS model of the RF filter which has been split down the symmetrical plane to reduce convergence time, the inset shows a closer view.

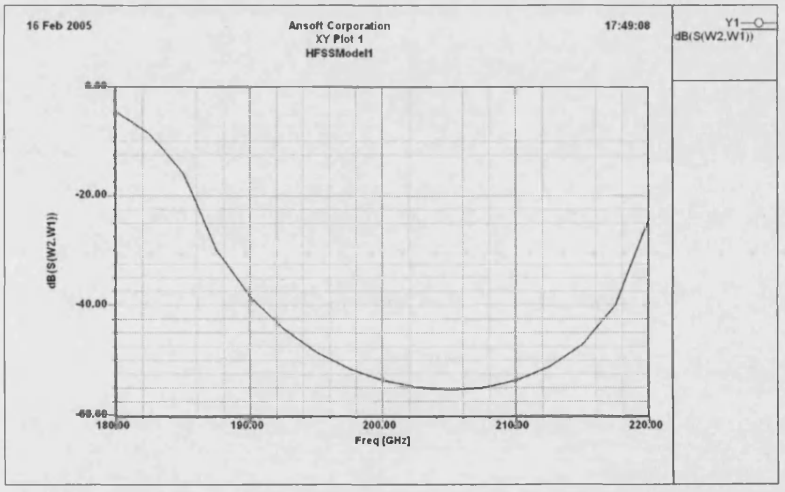


Fig. 5.16 Showing the frequency response of the RF filter in the band between 180 and 220 GHz.

5.3.3 Parasitic Modes

Many modes of the output frequency are supported by the input waveguide at full height. Since the second harmonic frequency is generated in the input guide it is possible that the signal will couple and propagate into the input guide. According to Porterfield, [5.5], the lowest order of these modes is the TM_{11}. It was important to

ensure that all these unwanted modes were cut-off in the input waveguide and this was done by sufficiently reducing the height.

The cut off frequency for a given waveguide mode (e.g. TE_{mn}) in a waveguide with dimensions a x b where b is the waveguide height is given by [5.6]

$$f_c = \frac{c}{2\pi}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \tag{5.3}$$

where c is the speed of light and m and n are the waveguide mode indices. From (5.3) all the possible waveguide modes for a full height WR10 waveguide can be calculated and some are shown in Table 5.1. Table 5.1 shows the TM_{11} mode is not cut off in a full height WR10 waveguide (2.54 x 1.27 mm) and is therefore supported to propagate freely at the output frequency. Table 5.1 also shows the cut off frequencies for the reduced height WR10 waveguide (2.54 x 0.30 mm). Table 5.1 indicates that the reduction in waveguide height has set the TM_{11} mode cut off frequency to 243 GHz. Any TM_{11} mode output frequencies generated in the input waveguide will certainly be in the cut off band and not supported, restricting output frequencies to the output circuit.

Mode	Mode indices		Full Height	Reduced Height
	m	n	$f_{c,full}$	$f_{c,red}$
TE_{10}	1	0	59	59
TE_{20}	2	0	118	118
TE_{30}	3	0	177	177
TE_{01}	0	1	118	236
TE, TM_{11}	1	1	132	243
TE, TM_{21}	2	1	167	264
TE, TM_{31}	3	1	213	295
TE, TM_{40}	4	0	236	236
TE, TM_{41}	4	1	264	334

Table 5.1 Showing cut off frequencies for a full height ($f_{c,full}$) (2.54 x 1.27 mm) WR10 waveguide and for a reduced height ($f_{c,red}$) (2.54 x 0.30 mm) WR10 waveguide. Highlighted cells indicate supported mode.

The supported modes were checked using HFSS. Two models were used to do this, a full height WR10 guide and a reduced height guide. The waveguides were allocated wave ports at either end and they were sufficiently long so there was no interference between the ports. Therefore the waveguide lengths were set to three guided wavelengths. The ports were specified to determine the presence of up to the first 10 modes if they were supported and to sweep in the output frequency band. Table 5.2 shows the HFSS simulated S_{21} response of the WR10 full height waveguide for the first 10 modes in the frequency range 190 – 210 GHz. It can be seen from Table 5.2 that the first six modes with the lowest cut off frequency, indicated by the shaded cells in column $f_{c,full}$ in Table 5.1, propagate without impedance and the TM_{11} is in this group. The table also suggests that two other modes are propagating with about 5 dB loss per λ_g of waveguide. Table 5.3 shows the HFSS simulated S_{21} response of the 2.54 x 0.30 mm (WR10 reduced height) waveguide for the first 10 modes in the frequency range 190 – 210 GHz. The table shows only three modes now supported which are indicated by the shaded cells in column $f_{c,red}$ in Table 5.1. In this case the TM_{11} mode is sufficiently suppressed.

Frequency	**Magnitude S_{21} data for Waveguide Modes (dB)**									
(GHz)	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*
190	0	-15	-15	0	0	0	0	0	-131	-120
192	0	-15	-15	0	0	0	0	0	-129	-120
194	0	-15	-15	0	0	0	0	0	-126	-119
196	0	-15	-15	0	0	0	0	0	-124	-119
198	0	-15	-15	0	0	0	0	0	-122	-119
200	0	-15	-15	0	0	0	0	0	-119	-118
202	0	-15	-15	0	0	0	0	0	-117	-117
204	0	-15	-15	0	0	0	0	0	-116	-115
206	0	-15	-15	0	0	0	0	0	-110	-106
208	0	-15	-15	0	0	0	0	0	-88	-87
210	0	-15	-15	0	0	0	0	0	-65	-64

Table 5.2 S_{21} data of propagating modes in full height WR10 waveguide.

Frequency	Magnitude S_{21} data for Waveguide Modes (dB)									
(GHz)	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*
190	0	0	0	-145	-153	-141	-143	-139	-148	-149
192	0	0	0	-145	-151	-139	-143	-139	-150	-151
194	0	0	0	-144	-149	-137	-144	-140	-152	-157
196	0	0	0	-144	-147	-137	-146	-140	-156	-169
198	0	0	0	-144	-146	-136	-149	-141	-159	-155
200	0	0	0	-144	-145	-136	-151	-141	-156	-149
202	0	0	0	-143	-145	-137	-149	-141	-152	-146
204	0	0	0	-142	-146	-138	-145	-140	-149	-143
206	0	0	0	-141	-147	-139	-142	-139	-147	-142
208	0	0	0	-140	-148	-140	-140	-138	-145	-140
210	0	0	0	-139	-150	-142	-138	-137	-144	-139

Table 5.3 S_{21} data of propagating modes in reduced height WR10 waveguide.

5.4 Multiplier Embedding Impedance

The embedding impedance can be defined as the impedance of the entire multiplier circuit as seen between the terminals of the diode as shown in Fig. 5.17. The embedding structure is passive and consists of transmission lines, backshorts and filters. Determining the embedding impedance allows the linear and nonlinear components of the multiplier to be analysed separately and is discussed further in Chapter 6.

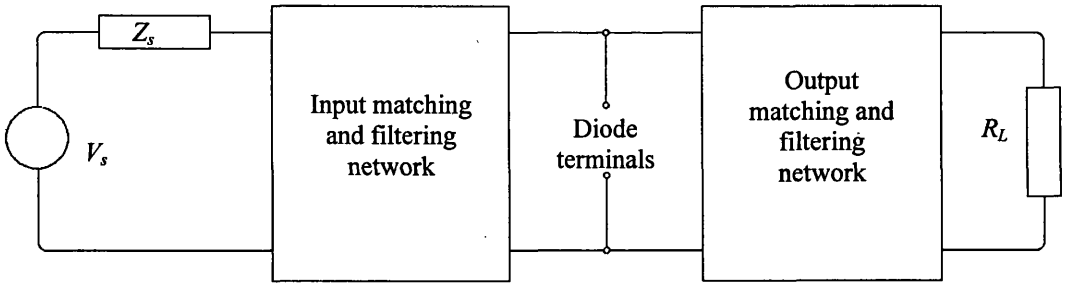
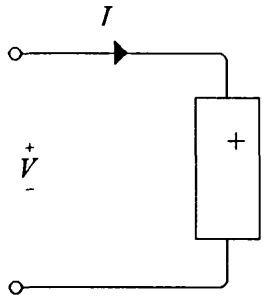


Fig. 5.17 Simplified circuit schematic of a multiplier indicating the terminals where a non-linear element such as a diode would be connected. The embedding impedance is measured between these terminals.

5.4.1 Diode Anti-Series Circuit Considerations

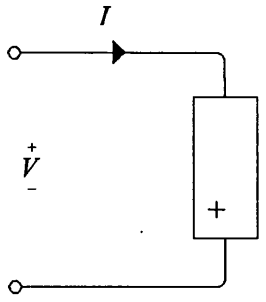
To fully understand how the embedding impedance should be interpreted for a single diode case, the anti-series diode pair configuration should be analysed. Consider first the following current relations for a two terminal nonlinear device. The I/V characteristics of a nonlinear device can be represented by a power series. The I/V characteristics are non-symmetrical hence the indication of the polarity of the device is shown. The current approximation for the first equivalent circuit is shown in Fig. 5.18.



$$I = f(V) = a_1 V + b_1 V^2 + c_1 V^3 + d_1 V^4 .... \qquad (5.4)$$

Fig. 5.18 Equivalent circuit and I/V approximation for single nonlinear device where I is the current that passes through the device, V is the voltage and a_1, b_1, c_1, d_1, are constants.

When the poles of the nonlinear device are switched but the source voltage orientation is maintained the equivalent circuit and corresponding I/V approximation are altered as shown in Fig. 5.19.



$$I = -f(-V) = a_1 V - b_1 V^2 + c_1 V^3 - d_1 V^4 ... \qquad (5.5)$$

Fig. 5.19 Equivalent circuit and I/V approximation for single nonlinear device with switched poles.

When in an anti-series pair the nonlinear devices are symmetrical about a common load, the output circuit in this case. The circuit representation for the anti-series pair is show in Fig. 5.20. Here A and B are two nonlinear devices (with marked polarity)

that pass currents I_A and I_B respectively, Z_{emb} represents the embedding impedance. The load current, I_L, passes through the output load denoted by R_L.

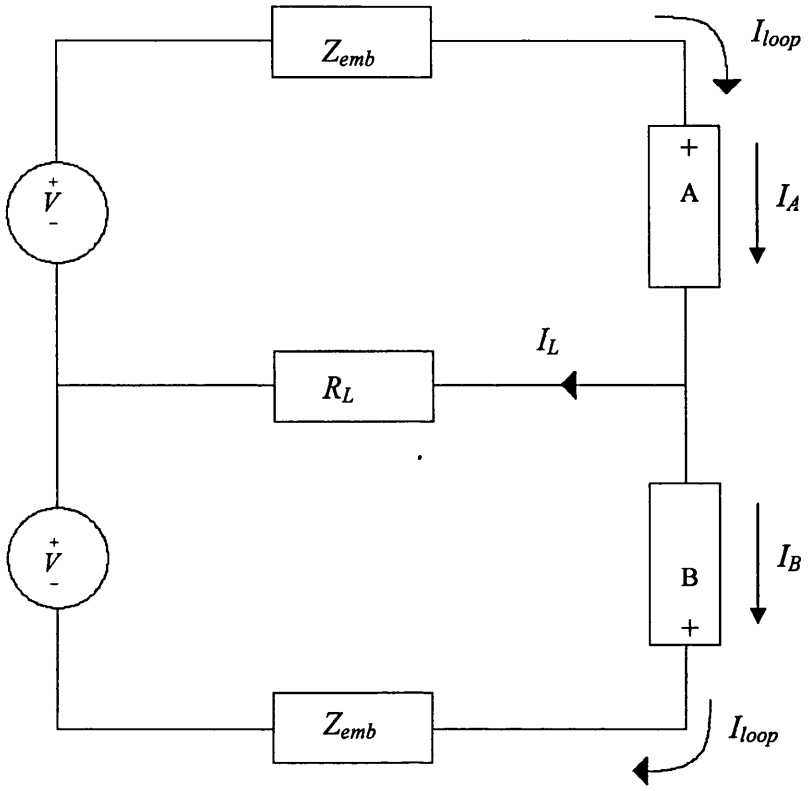


Fig. 5.20 Circuit schematic of the anti-series diode configuration which is symmetrical about the load R_L.

The current I_A can be described by (5.4) and the current I_B by (5.5) and therefore the current I_L is

$$I_L = I_A - I_B = 2b_1V^2 + 2d_1V^4... \tag{5.6}$$

which shows only even order voltage harmonics across the output load. The current in the outer loop is given by

$$I_{loop} = I_A = I_B = a_1V + c_1V^3... \tag{5.7}$$

which indicates odd order harmonics are confined to the diode loop and do not appear across the load and hence output circuit. In order to implement the harmonic balance code a representative circuit of a single nonlinear device is required. This is done by scaling the load and splitting the circuit as shown in Fig. 5.21.

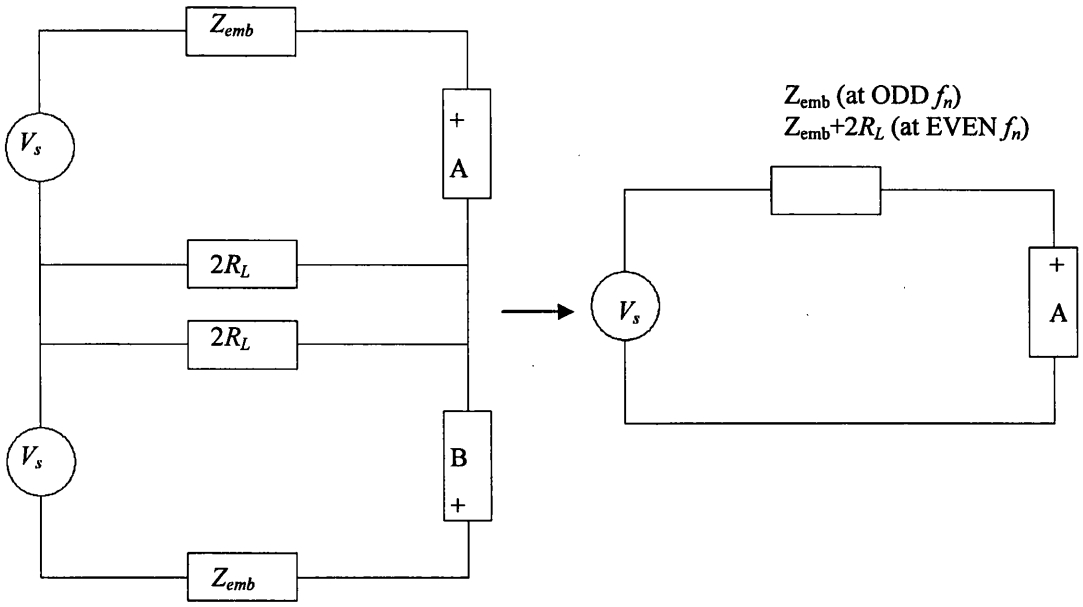


Fig. 5.21 Scaling and splitting the circuit to give an equivalent circuit containing one nonlinear element.

Current at odd order frequencies will flow through the outer loop of the circuit in Fig. 5.21. However, no odd order voltage will be dropped across R_L which effectively shorts the top loop of the circuit at odd harmonics. Therefore at odd harmonics the embedding impedance will be Z_{emb}. The even harmonics pass through the load which is doubled in value for the single device equivalent circuit. Hence the total impedance seen by the device at even harmonics is $Z_{emb} + 2R_L$.

5.4.2 Determining Embedding Impedance

The following section describes a very simple HFSS model of the multiplier structure constructed with little experience in using FEA packages. No account had been made for the diode structure or other details that arose from the actual fabrication process. A more detailed approach is given later.

Many researchers use finite element analysis packages, such as Ansoft's HFSS, to determine the embedding impedance of their passive networks, [5.5], [5.7]. There are two main routes of extracting this information; using a *lumped element gap source* and deembedding from a coaxial probe using a *wave port*. The coaxial probe method involves drawing a coaxial line into the computer model. The inner conductor is connected to one of the terminals and the outer to the other. The

embedding impedance is extracted from deembedding the reflection coefficient data down the coaxial line to the electrical position of the device. The other method is to use a lumped element gap source which acts as a miniature wave port between two conductors. An HFSS model showing a gap source with a calibration line is shown in Fig. 5.22.

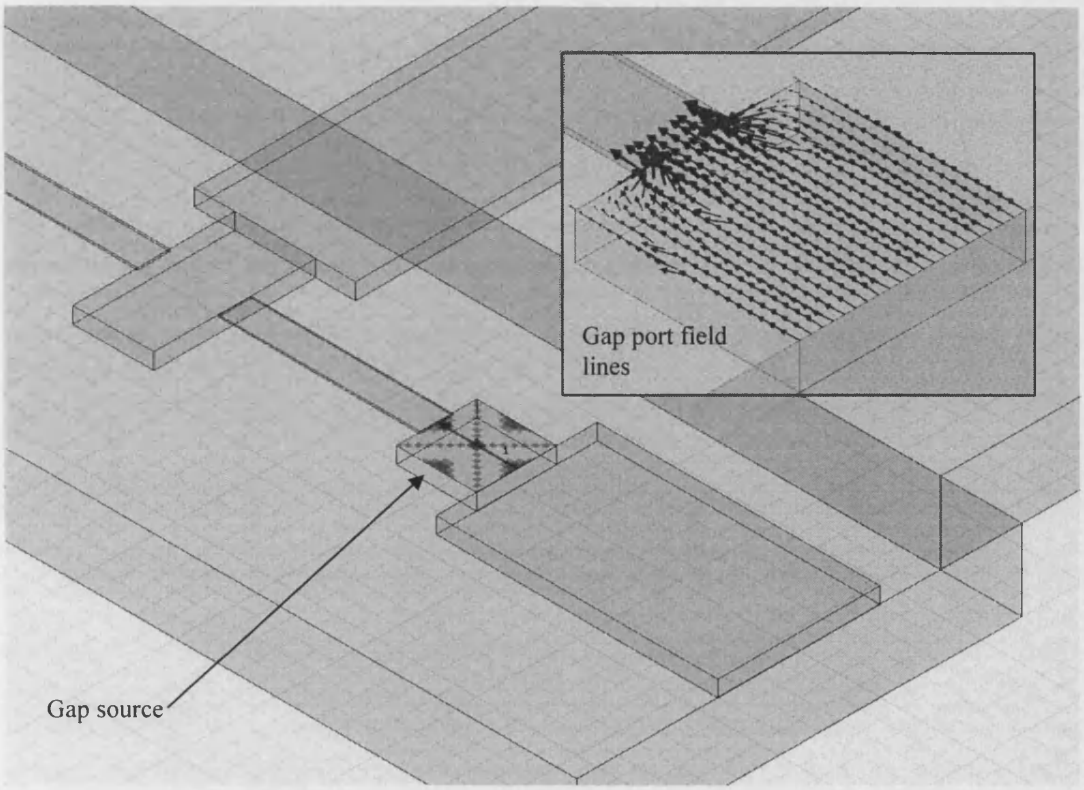


Fig. 5.22 HFSS model showing the gap source as a 2D square where an impedance line has been set indicated by the red arrow, inset shows port E field lines.

The gap source is a valuable tool for the RF engineer as it allows a versatile approach to designing and optimizing RF systems. The gap source can be used as a port where a complex impedance can be allocated to determine coupling efficiencies from other ports through a simulated network. The gap source can also be used to determine the embedding impedance. The complex reflection coefficient, Γ, at the diode terminals looking into the circuit will be [5.6],

$$\Gamma = \left(\frac{Z_{emb} - Z_g}{Z_{emb} + Z_g} \right) \tag{5.8}$$

where Z_g is the gap impedance. The equation (5.8) can be arranged for embedding impedance as a function of Z_g and complex reflection coefficient given by

$$Z_{emb} = Z_g \frac{(1+\Gamma)}{(1-\Gamma)}. \tag{5.9}$$

5.4.3 Embedding Impedance Consistency

As stated previously, calculated the embedding impedance is an important step in determining the multiplier efficiency. For this reason and general unfamiliarity with the HFSS modelling package at the time, several experiments were designed to look for consistency in the embedding impedance calculations.

5.4.3.1 Gap Source Impedance Z_g

The first test was to confirm that Z_{emb} was constant with changes in the gap source impedance Z_g. This was simply done by allocating different values to the gap source impedance and using the reflection coefficient and (5.9) to determine Z_{emb}. The complex components of Z_{emb} were then plotted as a function of Z_g as shown in Fig. 5.23. The results show minimal variation in Z_{emb} and any deviation from a perfectly straight line possibly arises from the non-convergence of the model.

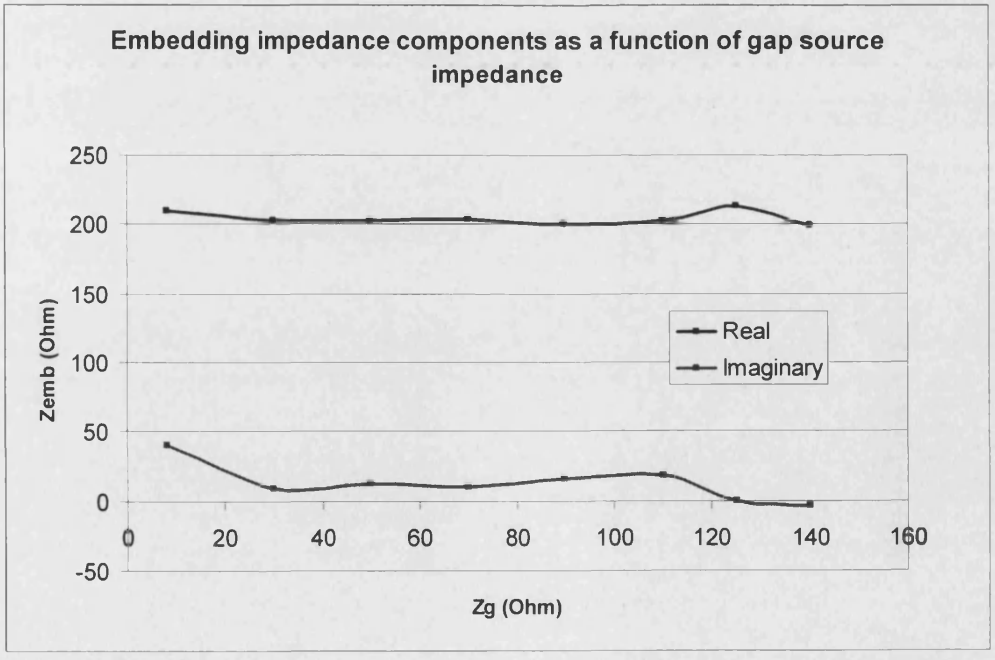


Fig. 5.23 Showing the consistent results of Z_{emb} as a function of gap source impedance Z_g.

5.4.3.2 Gap Source Height h_g

The height of the gap source above the substrate, h_g, was also investigated for consistency. The microstrip in the model was allocated 4 μm in height to account for the highly conductive n^+ layer that would not be removed under the microstrip during processing. For the purpose of this experiment the air bridge to the anode was replaced by a solid conductor. The height, h_g, was controlled by adjusting position of the 2D surface between the conductors as shown in Fig. 5.24. The results for Z_{emb} as a function of h_g for three different frequencies (80, 100 and 120 GHz) are shown in Fig. 5.25. The results clearly show that h_g has no effect on Z_{emb} at these frequencies.

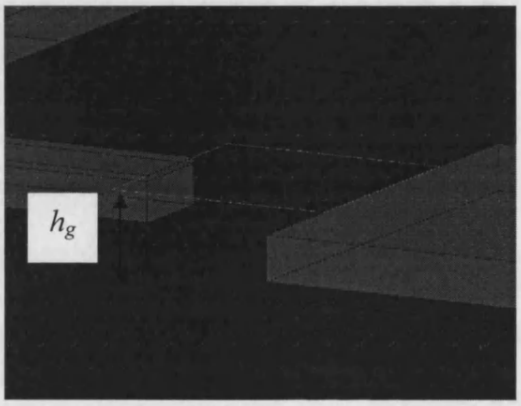


Fig. 5.24 Model of 2D gap source above substrate at height h_g between the 4um thick conductors on the semi-insulating gallium arsenide membrane substrate.

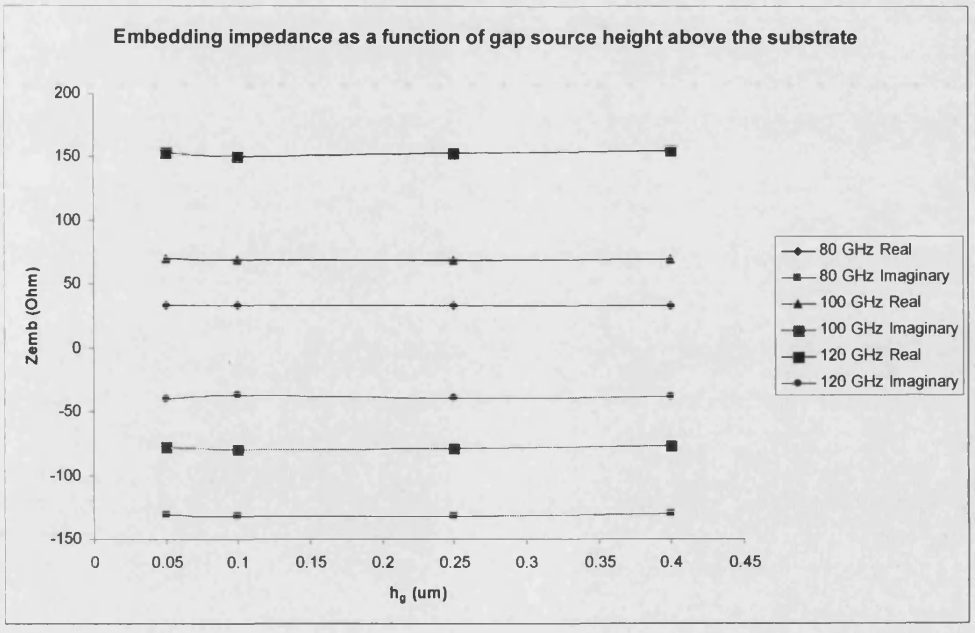


Fig. 5.25 Embedding impedance as a function of the gap source height above the substrate, h_g, covering three sections of the frequency band concerned. Lines between data marks are for visual aid only.

5.4.3.3 Lateral Gap Source Position l_g

The variation of embedding impedance as a function of lateral position across the membrane (parallel to the E field), l_g, was investigated. An HFSS model similar to that in Fig. 5.3 was used replacing the pair of gap sources for a single one that could be moved across a single piece of conductor. A parametric sweep was used to move the gap source across the conductor for two frequencies to look for any dramatic change in embedding impedance. The results of the parametric sweep are shown in Fig. 5.26 for 100 GHz and Fig. 5.27 for 200 GHz.

The information in Fig. 5.26 and Fig. 5.27 is useful for matching and tuning the embedding impedance to the diode impedance. Obviously there will be limitations to this tuning ability governed by the physical size of the diodes.

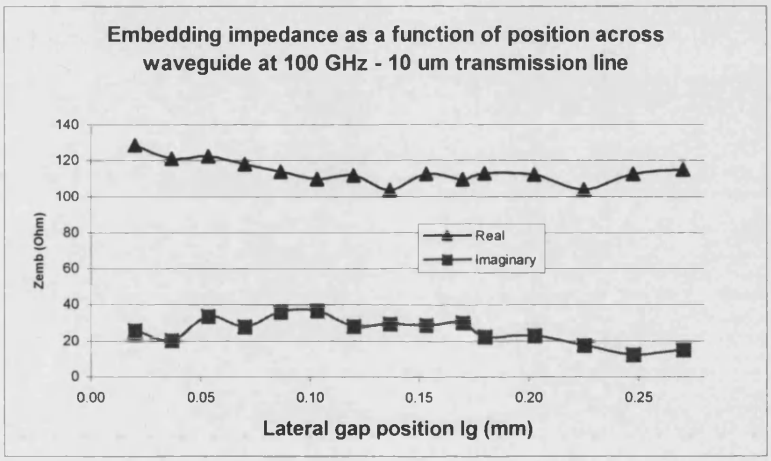


Fig. 5.26 Embedding impedance as a function of l_g at 100 GHz for a 10 μm feed line GHz.

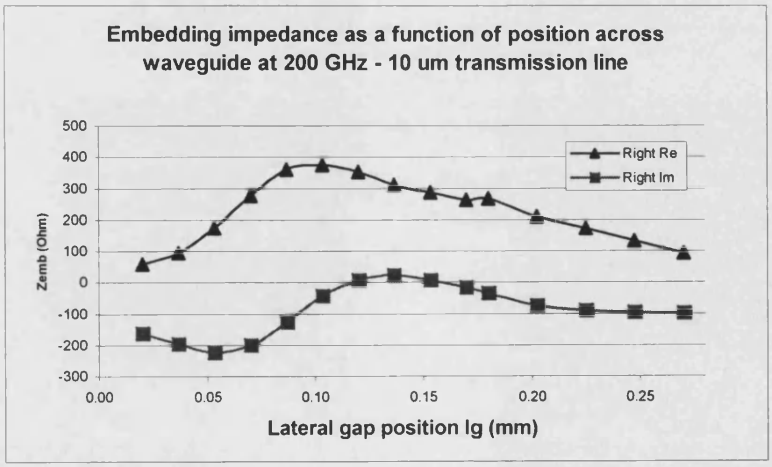
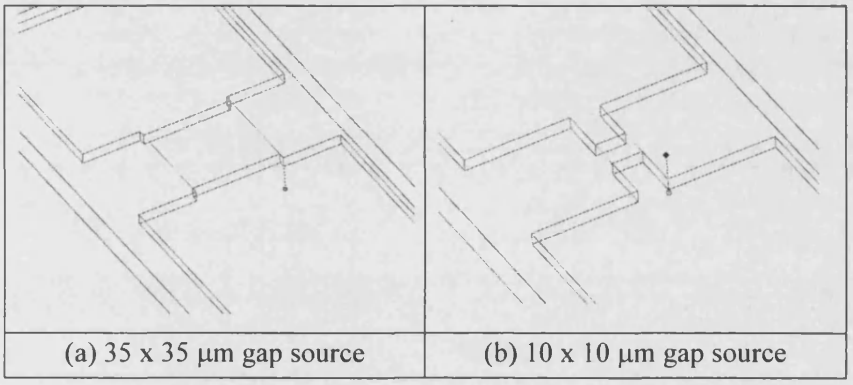


Fig. 5.27 Embedding impedance as a function of l_g at 200 GHz for a 10 μm feed line.

5.4.3.4 Gap Source Area A_g

The effect of the gap source area, A_g, on the embedding impedance was also of concern from a design point of view. If the gap source area had an influence on Z_{emb} then its position and size would both be crucial and the gap source geometry would have to be refined from the simple 2D square. An example to illustrate the gap source geometry is shown in Fig. 5.28. The results of varying the gap source area whilst maintaining its central position and aspect ratio is shown in Fig. 5.29. The results show the embedding impedance is independent of gap source area.



(a) 35 x 35 μm gap source | (b) 10 x 10 μm gap source

Fig. 5.28 Showing examples of (a) 35 x 35 um gap source and (b) 10 x 10 um gap source maintaining the central position.

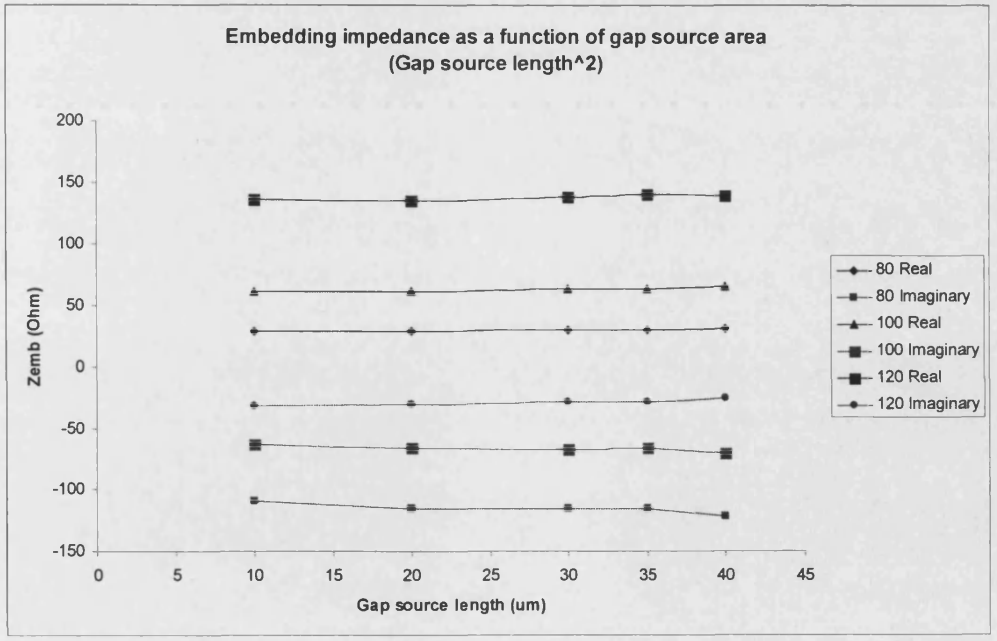


Fig. 5.29 Embedding impedance as a function of gap source area for three frequencies; 80, 100 and 120 GHz. Data points are connected by a line purely as a visual aid.

5.4.3.5 Height of Membrane, h_m, in Waveguide

The vertical height of the entire membrane, h_m, in the input waveguide was varied and its effect on the embedding impedance analysed. Fig. 5.30 illustrates the variable h_m in a HFSS model. The value for h_m was set to zero at exactly half of the height of the input waveguide (1.27 mm) and the deviation from zero varied. Fig. 5.31 shows the embedding impedance as a function of membrane height deviation (from centre) in the guide at a frequency of 100 GHz and at 200 GHz in Fig. 5.32. This information shows the relative height independence of embedding impedance at 200 GHz and only a slight variation at 100 GHz. For ease of fabrication of the multiplier block, h_m was maintained at zero.

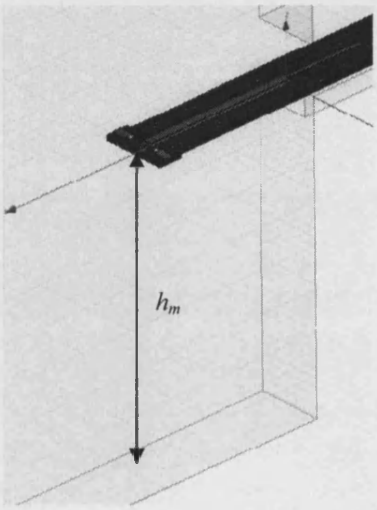


Fig. 5.30 Showing the membrane height in the waveguide h_m.

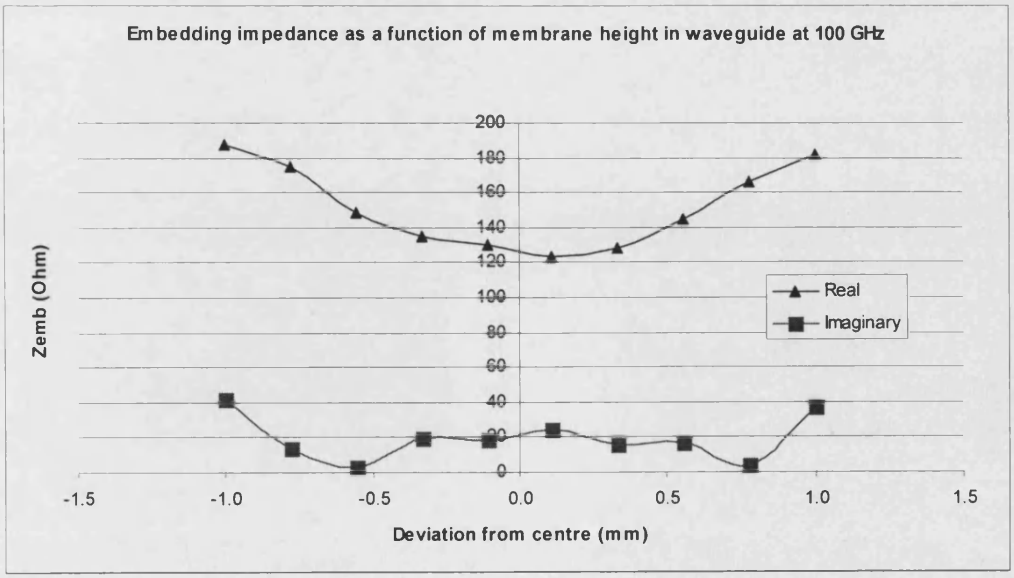


Fig. 5.31 Embedding impedance as a function of h_m at 100 GHz.

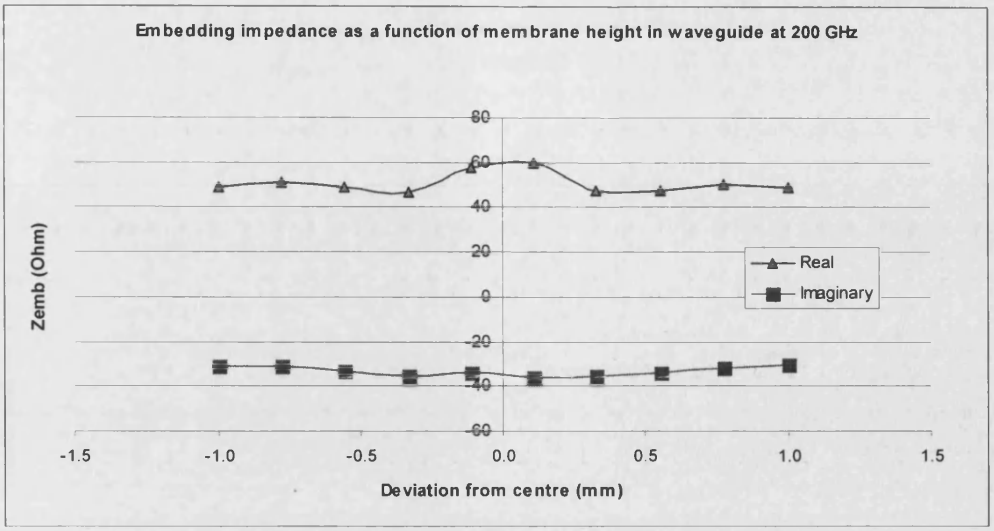


Fig. 5.32 Embedding impedance as a function of membrane height in the input waveguide at 200 GHz.

5.4.3.6 Effective Backshort Position L_{eff}

The effective backshort position, as shown in Fig. 5.7, will obviously have the most profound influence on the embedding impedance. The embedding impedance as a function of L_{eff} is shown in Fig. 5.33 in (a) Cartesian form and (b) on a Smith chart. The plot illustrates the cyclic behaviour of the embedding impedance as the backshort is taken through $\lambda_g/2$.

The value of L_{eff} is effectively the position of the terminating backshort wall with respect to the position of the gap source and, hence, will directly determine the reactance seen there. The reactance is essentially determined by the imaginary component of the embedding impedance and can be tuned to be positive (inductive) or negative (capacitive) which is of great benefit in providing an impedance match to the diodes. The varactor diodes that will be positioned in place of the gap source will effectively see this reactance as a parallel component. This can be used advantageously to tune the circuit.

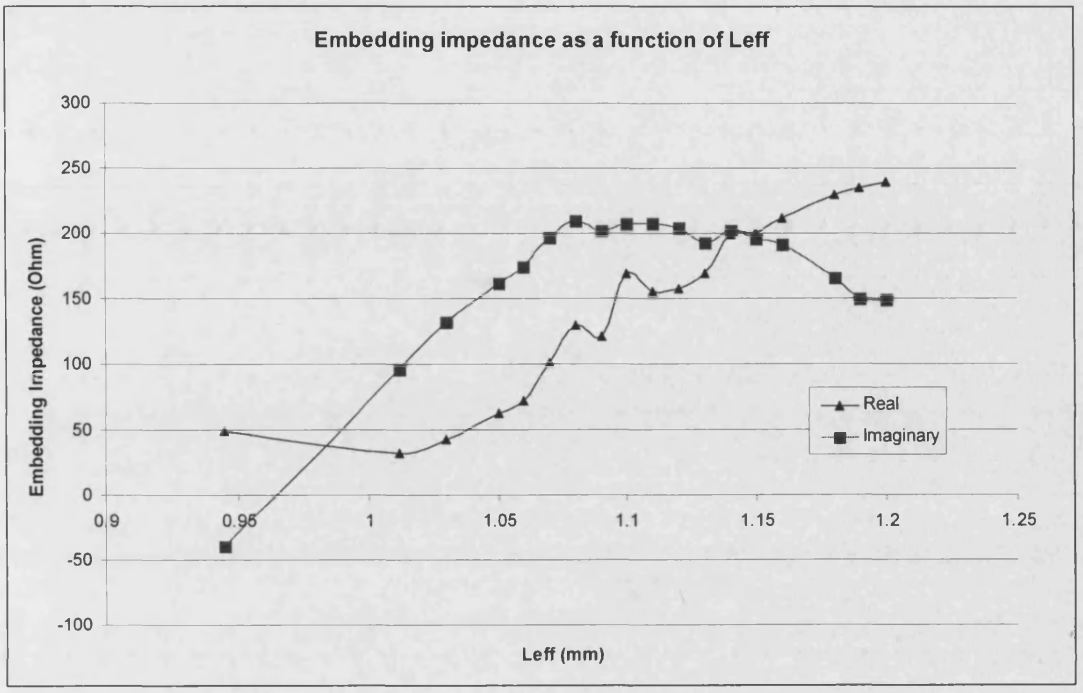


Fig. 5.33(a) Cartesian plot of embedding impedance as a function of L_{eff} at 100 GHz.

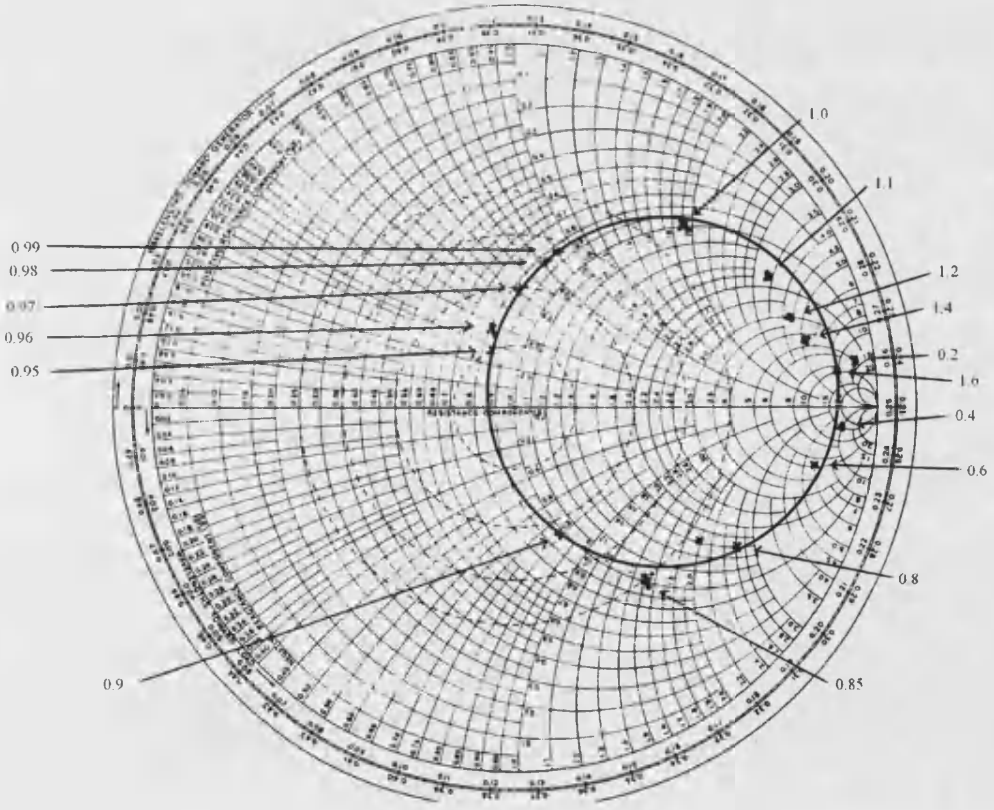


Fig. 5.33(b) Embedding impedance as a function of L_{eff} at 100 GHz plotted on a Smith chart.

5.4.4 Scale Model Embedding Impedance

A scale model is the conventional method used to determine the embedding impedance of a high frequency structure, [5.8], [5.9]. A small coaxial line is placed in the scale model with the inner and outer conductor each connected to a different terminal of the device junction. Using standard network analysing equipment it is important to account for the shift in phase that is needed as a result of the extra length of transmission line. This is corrected by shorting the end of the transmission line and adjusting the phase offset for each required frequency. The S_{11} is then measured using the phase correction and the embedding impedance can be determined from this, usually normalised to 50 Ω.

A scale model of a simple mixer structure was used to take values of embedding impedance as a function of backshort position. The mixer structure was then modelled in HFSS to compare results between the two methods. A Smith chart plot of the measured and modelled embedding impedance as a function of backshort position at 4 GHz is shown in Fig. 5.34. The correlation between the two sets of data is not perfect. This was due to imperfections in the real model that were not accounted for in the HFSS model, i.e. perfect backshort and no gaps in the metal side walls.

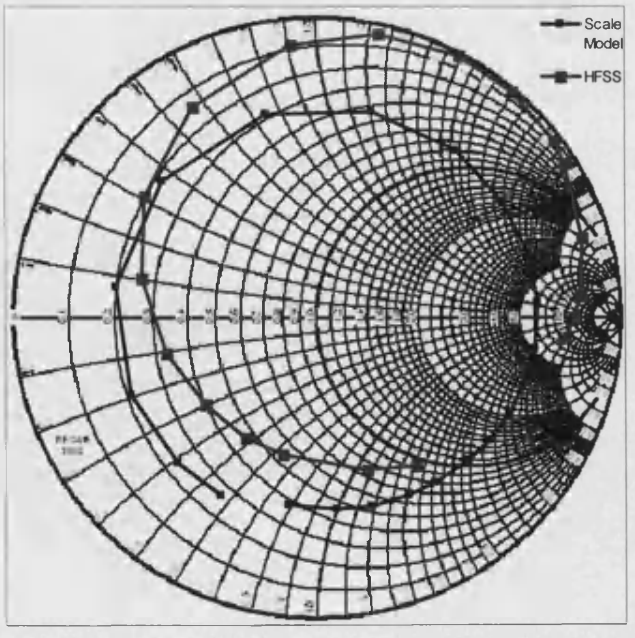


Fig. 5.34 Smith chart plot of the embedding impedance as a function of backshort position at 4 GHz for the measured and modelled mixer structure.

5.5 Scale Model Multiplier

It was decided to use some commercial diodes inside the scale model to simulate the working of the multiplier. The HFSS modelling was used to calculate the effective backshort position for the scale model and a mock substrate was made at the scaled size. This calculated backshort length obviously did not take into account that the diodes would alter the impedance of the microstrip probe and therefore this model would not be truly optimised. The scale model obviously had a fixed value of the effective input backshort position but a tuneable output backshort was constructed using a sliding aluminium block on a threaded post. Two of the commercial diodes were placed on the substrate and contacted to the copper substrate using a silver conducting paint. The input and output guides were bolted to the split block of aluminium that contained the microstrip cavity and moving output backshort. Fig. 5.35 shows a photograph of the scale model multiplier with the top half of the microstrip cavity block and input waveguide lid removed. The gallium arsenide substrate with the adhesive copper microstrip tracks can also be seen in Fig. 5.35 with arrows indicating the location of the diodes.

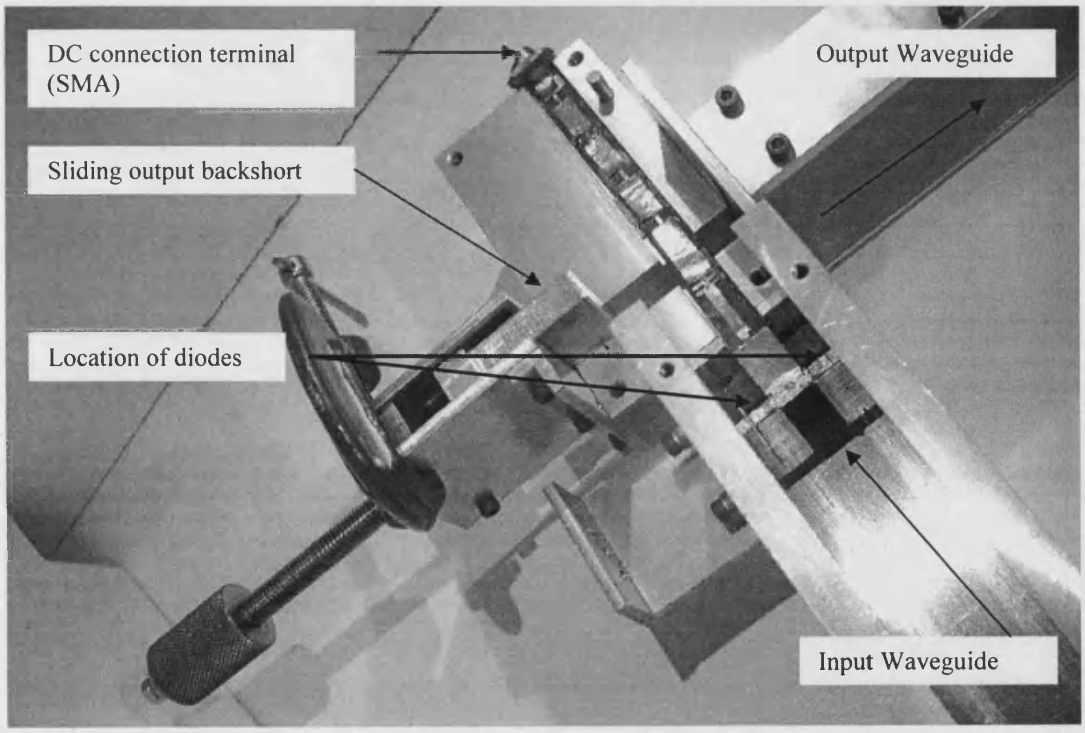


Fig. 5.35 Photograph of the scale model multiplier with the top half of the cavity block and input guide lid removed.

The multiplier input signal was generated from a network analyser which was amplified to give a maximum input level of 1000 mW (30 dBm). A DC power source provided up to 9.9 V to bias the diodes and a spectrum analyser was used to monitor the output of the multiplier.

It was initially found that a large amount of power at the output frequency was simply being transmitted to the DC terminal and not coupling down the output guide. This was due to the inferior RF filter made from the copper adhesive tape. This was replaced with a filter made using photolithography and gold evaporation techniques which gave much better results. Fig. 5.36 shows the transmission of output power as a function of frequency for the original and the modified filter design.

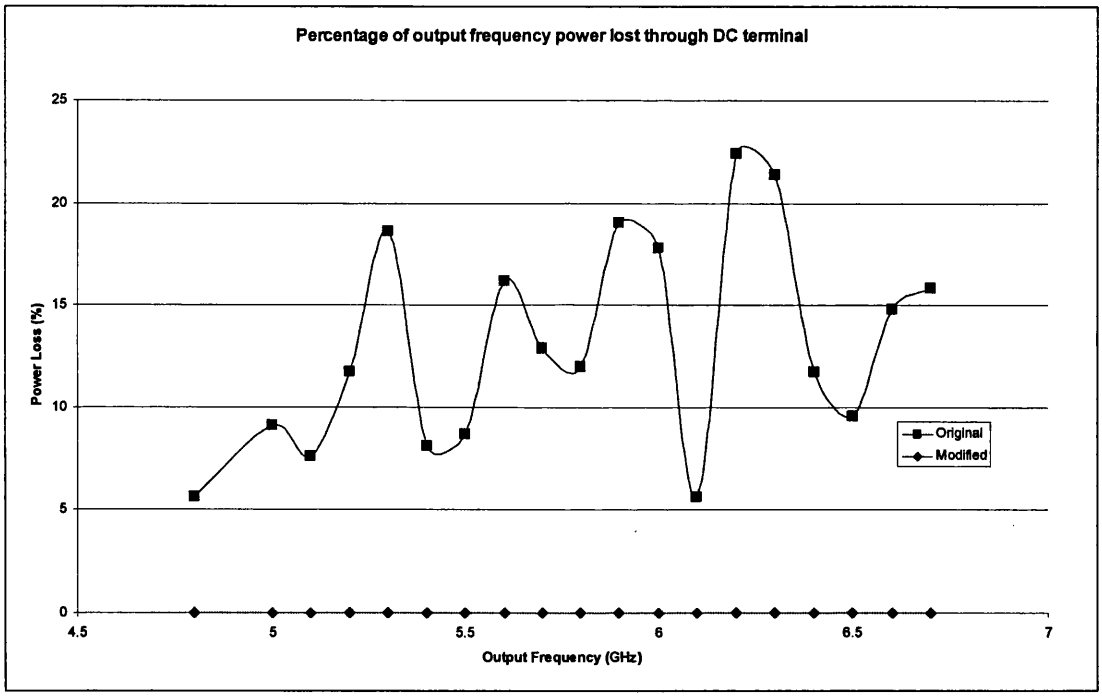


Fig. 5.36 Shows the percentage of output frequency power being transmitted through the DC terminal for the original and modified filters.

The optimum drive level of the scale model multiplier could be established by looking at the output level as a function of input level for a given frequency. For this experiment a frequency of 2.85 GHz was chosen and the results are shown in Fig. 5.37. The peak drive level at 2.85 GHz is at an input of 26 dBm which is approximately 400 mW. This would normally be far too much for high frequency multiplier but the diodes used in this scale model had a much larger anode area and

therefore could handle more power. The peak output power at an output frequency of 5.7 GHz was 23.4 mW (13.7 dBm). For each reading the output backshort was tuned and the diode bias was adjusted to give the best performance.

The effect of altering the diode bias with respect to the scale model efficiency was also investigated and the results are shown in Fig. 5.38. The diode voltage bias will adjust the effective impedance of the diode and hence allow fine tuning of the circuit. Essentially, the higher the bias (the bias is always reverse for a multiplier) the lower the capacitance of the diodes up to the breakdown voltage. Therefore it would be expected that the closer to breakdown the diodes are biased the more efficient they will be operating. Fig. 5.38 shows two very distinct areas in the graph structure where the output power is significantly low (at 3.5 V and 6 V). These points of low efficiency are probably due to unwanted resonance inside the multiplier.

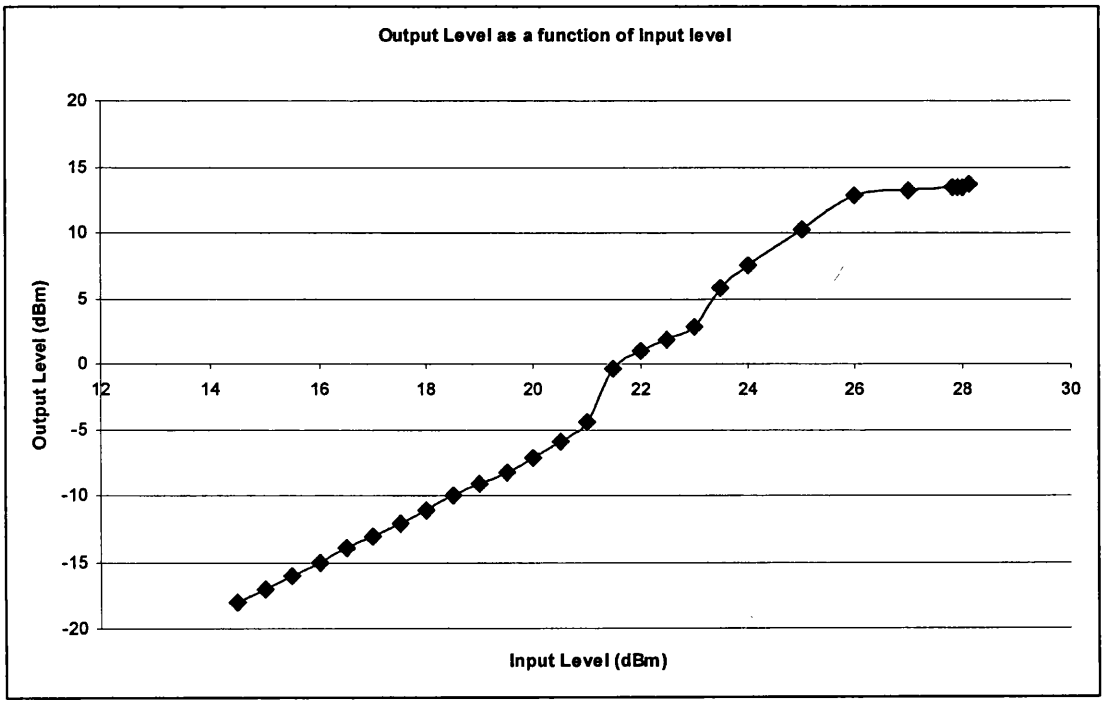


Fig. 5.37 Output level of scale model multiplier as a function of input drive level at an input frequency of 2.85 GHz.

Finally the frequency response of the multiplier was recorded at a fixed input power of 21 dBm which was the highest power level attainable across the entire input band. The results of the scale model conversion efficiency are shown in Fig. 5.39. The conversion efficiency of the scale model is relatively low but this was expected as no

matching to the diode was performed other than device biasing. There is much structure in the conversion loss graph which, again, probably arises from resonance within the multiplier structure or ripple in the source output. Much of the external loss for the network was also not accounted for in Fig. 5.39. The total loss of output power through the external cables was measured at ~1.7 dB.

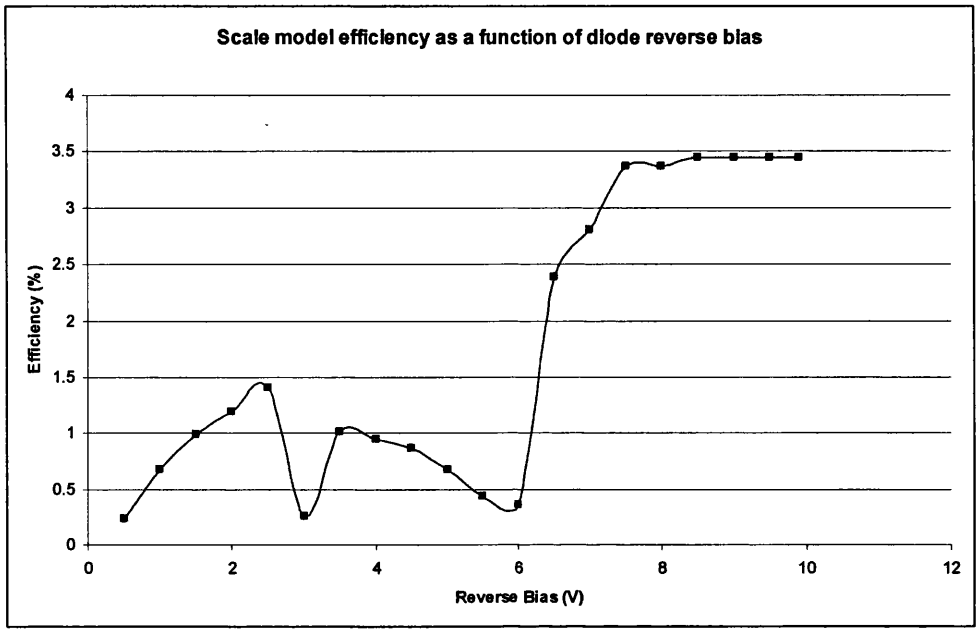


Fig. 5.38 Scale model efficiency as a function of diode reverse bias at an input frequency of 2.85 GHz.

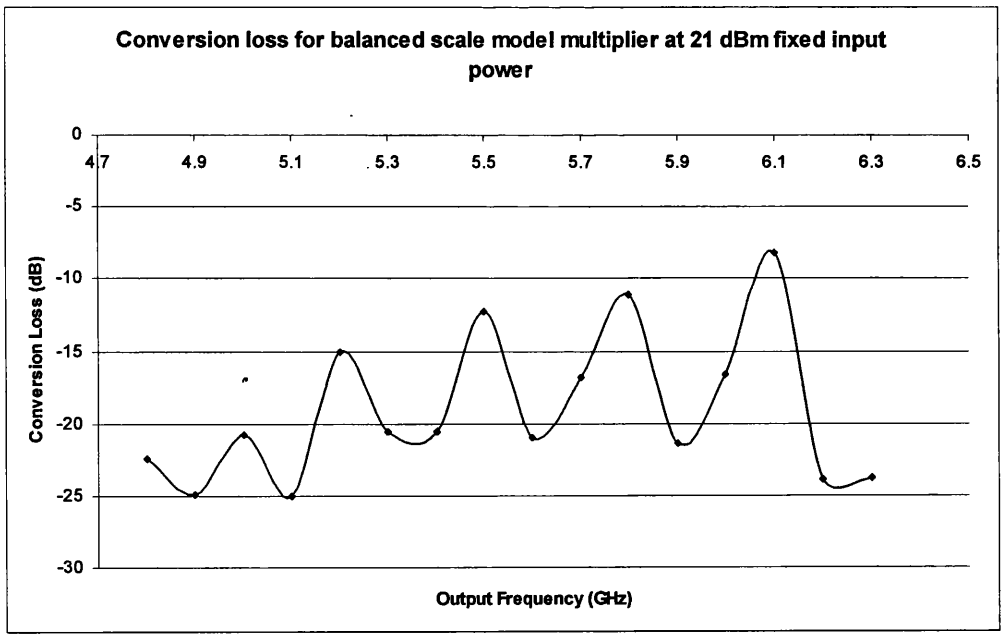


Fig. 5.39 Scale model conversion efficiency for the balanced harmonic doubler with two diodes in an anti-series configuration, reverse bias ~9 V. A data line is used between the points as a visual aid.

5.6 Advanced HFSS Model

The calculations of embedding impedance made in made in Fig. 5.33 were used in chapter 6 for determining the multiplier output power and efficiency. However, this structure was incomplete with regards to some aspects of the multiplier geometry, namely that of the diode structure. The embedding impedance and harmonic balance analysis need to work in harmony to incorporate a full picture of the multiplier circuit. What has not been discussed at this point is what the embedding impedance data should include for the harmonic balance program to work accurately.

5.6.1 Requirements from the Harmonic Balance Program

Up to this point the gap source has been modelled as a 20 x 20 μm 2D object, 4 μm above a semi-insulating gallium arsenide substrate. Between the two terminals of the gap source the rest of the diode would sit, i.e. a small section of finger contacting to the anode, some silicon dioxide passivation, n and n^+ doped gallium arsenide and a semi-buried ohmic contact. The harmonic balance program used in Chapter 6 only models the behaviour of the diode junction and a few components of the series resistance between the terminals. What was not included to a sufficient enough degree was a description of the parasitic capacitance seen by the diode. This included detail of the diode geometry and materials anywhere between the anode and the cathode. It was also reasonable at this point to include a few other adjustments to the model that would arise from the actual fabrication of the multiplier such as gold thickness, ohmic contact etch depth and any wet etch profiles that should be included.

It should be noted here that extra parasitic losses (such as the diode parasitic capacitance) were intended to be added manually to the embedding impedance found using the basic model to give a more realistic description of the multiplier behaviour. However the bulk of the diode parasitic component modelling was done after the completion of the basic modelling of the multiplier.

5.6.2 Modified HFSS Structure

An overview of the modified structure is shown in Fig. 5.40. The model now contained the correct finger length, width and expected gold thickness, the buried

ohmic contact and the layer structure of the gallium arsenide wafer. The silicon dioxide insulation layer was also included. The advanced model tried to match exactly how the multiplier chip was fabricated.

The model was parameterised so that everything viewed in Fig. 5.40 could move in and out of the input waveguide under command of a single variable. This simulated L_{eff} and again was crucial for the design optimization. The new model took considerably more time to solve than the previous basic model. This was because of the much smaller details present in the model. In some cases the entire central conductor (RF filter and transmission line to the fingers), insulator and conductive GaAs underneath it were combined as a single element and assigned as gold. This greatly reduced convergence time of the model. A step-by-step guide to how the advanced model was constructed is shown in Fig. 5.41.

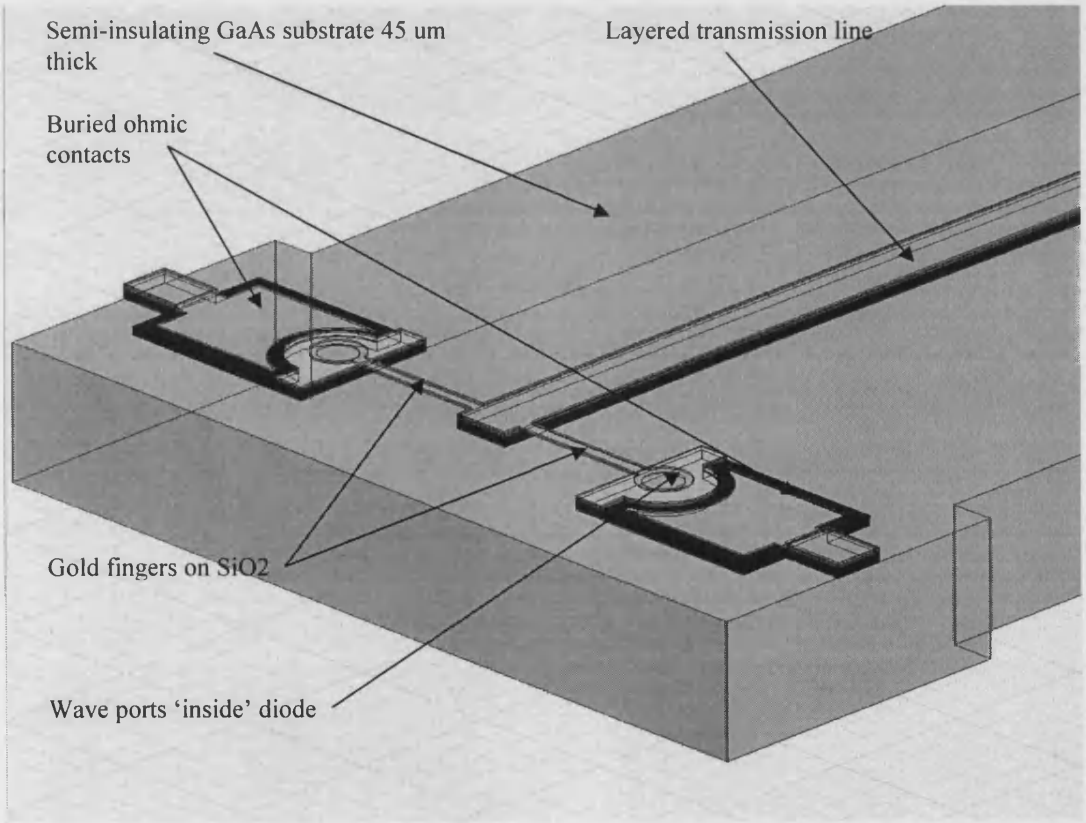


Fig. 5.40 Advanced HFSS model including more detail of the diode structure.

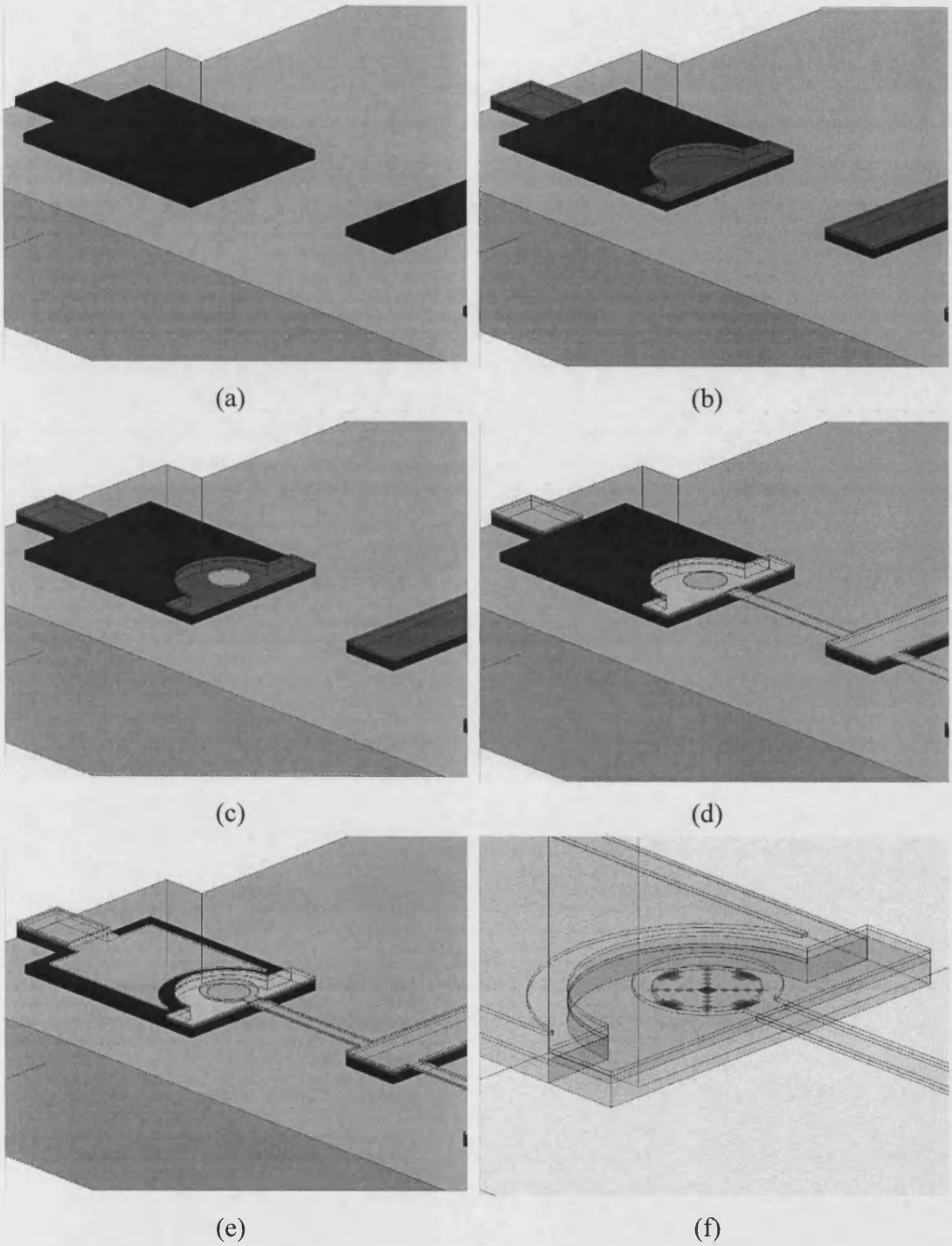


Fig. 5.41 A progressive construction of the HFSS diode model showing (a) the semi insulating GaAs substrate (grey) with the highly conductive n^+ layer (dark blue), (b) the n doped layer GaAs (light blue), (c) the anode (light grey), (d) the SiO_2 around the anode and under the fingers and microstrip, (e) the gold capping layer (yellow/ orange) and (f) the diode port situated underneath the anode (see later).

5.6.3 Modified Wave Port

The 2D circular wave port in the advanced model was situated directly between the anode and the n^+ material [5.10]. It was slightly larger in diameter than the anode by

approximately 10% and the port integration/ impedance line was set from the centre of the anode to the edge of the port. This is done to reduce spurious modes propagating in the model. The *n* gallium arsenide material from directly under the anode was removed as the information from this part of the diode circuit is described in the nonlinear analysis and should not be included in the embedding impedance. When resolving S_{11} parameters it was also important to normalise the port to a known impedance to be used when calculating Z_{emb}. An example of the anode port field lines is shown in Fig. 5.42.

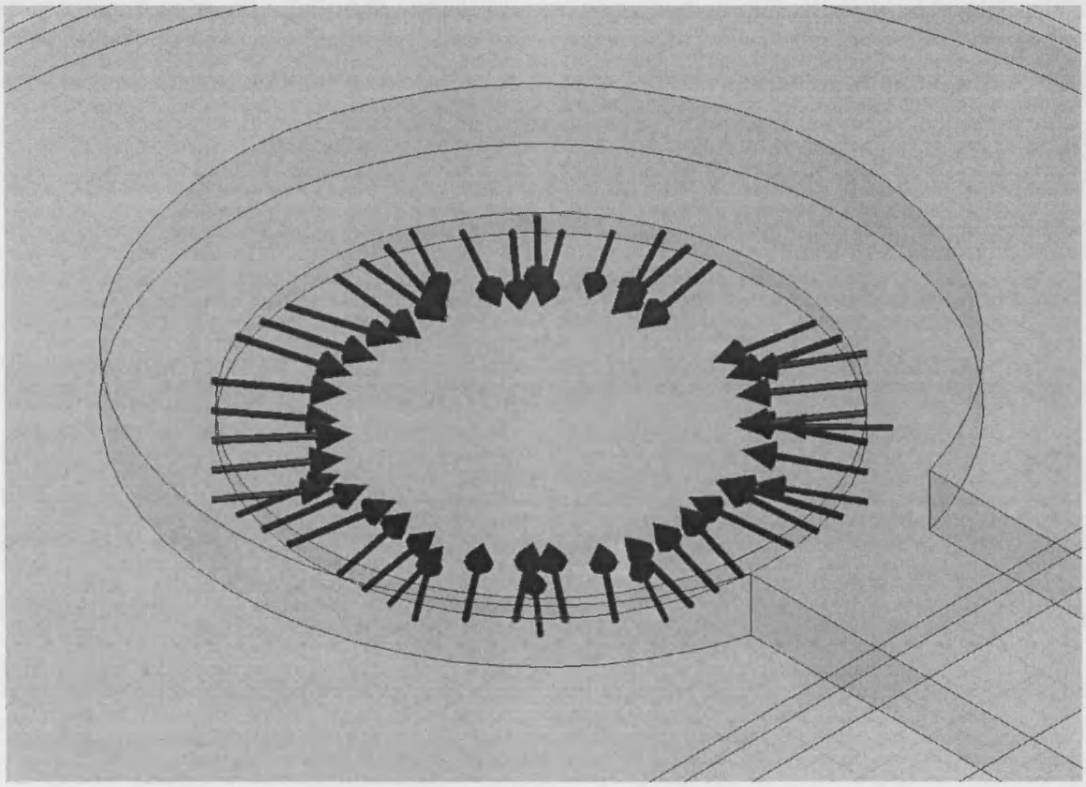


Fig. 5.42 HFSS representation of the anode wave port field lines set by the integration/ calibration line

The anode wave port could be assigned differently using a coaxial probe, [5.11]. The coaxial central conductor was simply an extension of the anode that penetrated the n^+ material and the dielectric is the *n* material. The wave port was deembedded to where the metal-semiconductor interface would be. A circuit schematic of the coaxial wave port is shown in Fig. 5.43.

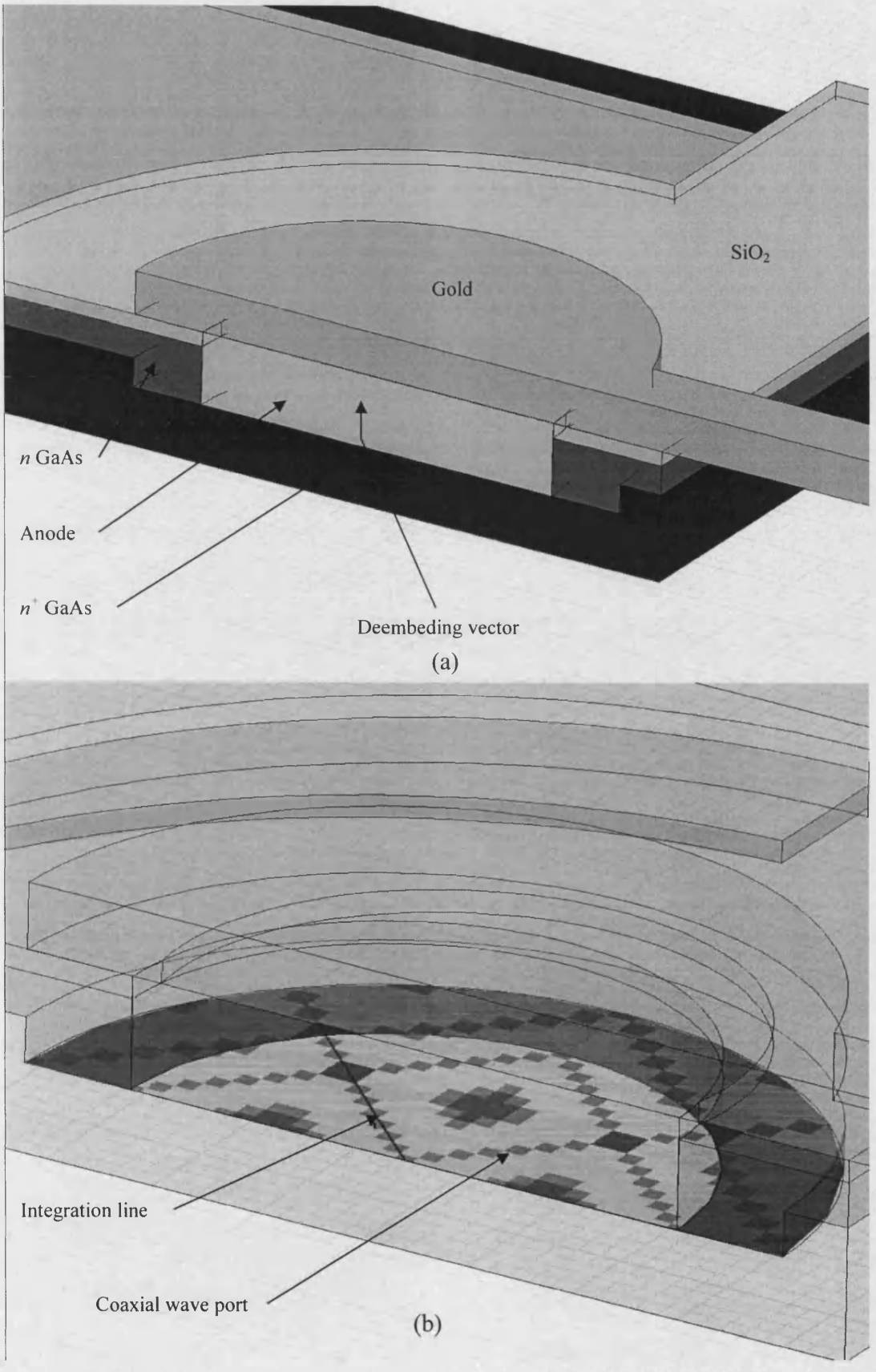


Fig. 5.43 Showing (a) a side view cross-section of the diode model used with the coaxial anode port method and (b) the wave port indicating the integration line.

5.6.4 Embedding Impedance of the Advanced Model

The embedding impedance of the advanced model was found using the planar anode wave port approach described above. The advanced model now included the details in the model that contributed to the parasitic capacitance. Therefore the imaginary components of the embedding impedance, as a function of L_{eff} say, were expected to contain more negative elements, i.e. a shift in the Smith chart downwards. A direct comparison between the two models in the same waveguide structure is shown in Fig. 5.44.

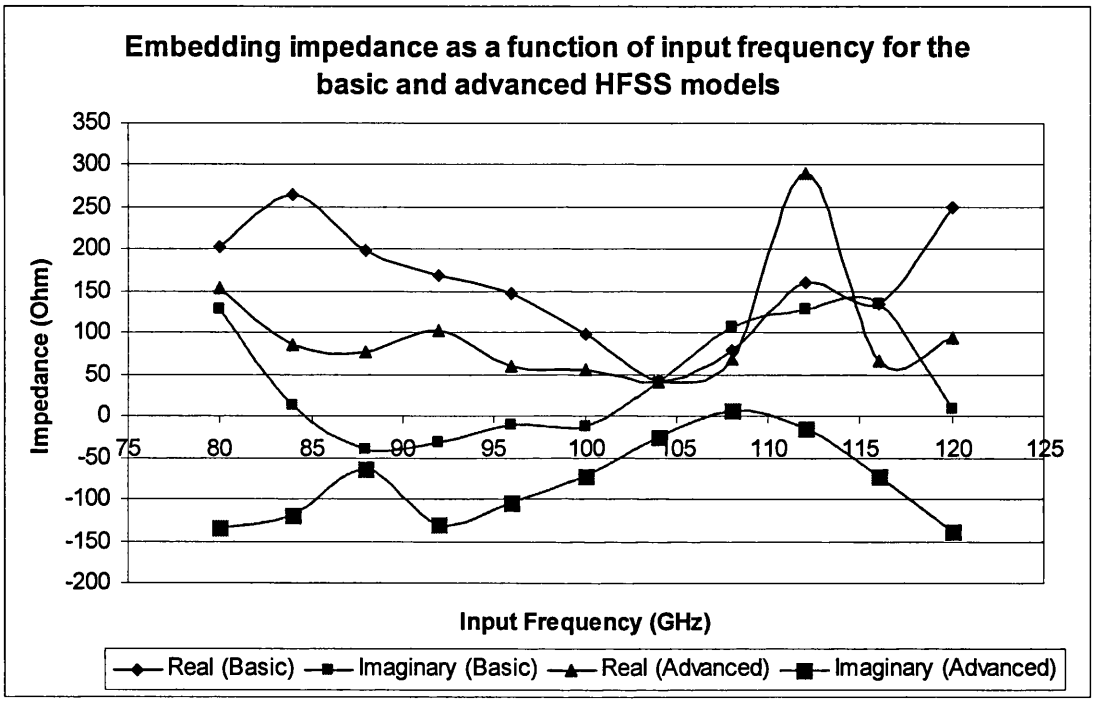


Fig. 5.44 Embedding impedances as a function of input frequency for the basic and advanced HFSS models with L_{eff} consistent.

Fig. 5.44 clearly shows the increase in the negative weighting of the imaginary components of embedding impedance in the advanced model compared to that in the basic model. The advanced model is describing a more realistic picture of the multiplier circuit although this will have an adverse effect on the performance of the multiplier efficiency. Power in the circuit will be lost through these parasitic components making less available for the multiplying effect in the diodes.

References – Chapter 5

[5.1] Y-C. Shih, *et al.*, "Waveguide-to-microstrip transmission for mm-wave applications," *Microwave Symposium Digest*, IEEE MTT-S International, vol. 1, May 1988, pp. 473-475.

[5.2] Y-C. Leong, S. Weinreb, "Full band waveguide-to-microstrip probe transitions," *Microwave Symposium Digest*, IEEE MTT-S International, vol. 4, June 1999, pp. 1435-1438.

[5.3] A. G. Williamson, "Analysis and modelling of "two-gap" coaxial line rectangular waveguide junctions," *IEEE Transactions on Microwave Theory and Techniques*, vol. MTT-31, no. 3, March 1983, pp. 295-302.

[5.4] J. A. Stratton, "Electromagnetic theory," McGraw-Hill, New York, 1941.

[5.5] D. W. Porterfield, *et al.*, " A high-power fixed-tuned- millimeter-wave balanced frequency doubler," *IEEE Trans. on Microwave Theory and Techniques*, vol. 47, no. 4, April 1999, pp. 419-425.

[5.6] D. M. Pozar, "Microwave engineering," John Wiley and Sons Inc., New York, 1998.

[5.7] W. Zhang, *et al.*, "Scaled model measurement of the embedding impedance of a 660-GHz waveguide SIS mixer with a 3-standard deembedding method," *IEEE Microwave and Wireless Components Letters*, vol. 13, no. 9, September 2003, pp. 376-378.

[5.8] C. E. Hagstrom, E. L. Kollberg, "Measurements of embedding impedance of millimeter wave diode mounts", *IEEE Transactions on microwave theory and Techniques*, vol. MTT-28, no. 8, August 1980, pp. 899-904.

[5.9] M. J. Feldman, S. K. Pan, A. R. Kerr, A. Davidson, "SIS mixer analysis using a scale model," *IEEE Transactions on Magnetics*, vol. mag-19, no. 3, may 1983, pp. 494-497

[5.10] A. Maestrini, B. Thomas, "Report on the evaluation of the capabilities of united monolithic semiconductors to produce Schottky based mixers in the band 100-380 GHz," UMS Report

[5.11] J. L. Hesler, *et al.*, "Fixed tuned submillimter wavelength waveguide mixers using planar Schottky barrier diodes," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 5, May 1997, pp. 653-658.

Chapter 6

Harmonic Balance Analysis

This chapter will use harmonic balance analysis to make predictions of the multiplier output power and efficiency. Two sets of predictions can be made using the basic and advanced HFSS multiplier structure models. The embedding impedance information in conjunction with the varactor diode modelling is implemented in the harmonic balance code modified for the purpose of this project and originally written by Siegel, Kerr and Hwang [6.1]. The code was originally intended as a mixer program but modified at the University of Bath to be used for a multiplier. Some basic optimisation of the multiplier can be carried out by modifying backshort positions and diode parameters.

6.1 Harmonic Balance Equation

The method used to derive the circuit equations implemented in the code is known as the piecewise technique proposed by Nakhla and Vlach [6.2]. This technique is a modification of an original method implemented by Baily [6.3] and Lindenlaub [6.4]. The original method required many variables to be optimized resulting in very large computational problems. The modifications made by Nakhla and Vlach limited the problem to the linear and nonlinear subnetworks. This required only frequency domain solutions for the linear subnetwork dramatically reducing computational time. Fig. 6.1 shows a circuit schematic of the multiplier circuit that has been modified to account for a single diode (see Chapter 5). This circuit can be rearranged to separate the linear and nonlinear components as shown in Fig. 6.2.

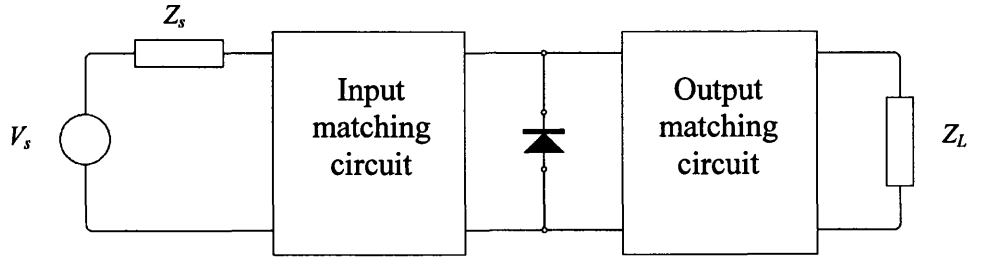


Fig. 6.1 Circuit schematic of the frequency multiplier using just a single diode, V_s and Z_s are the source voltage and impedance respectively and Z_L is the load impedance.

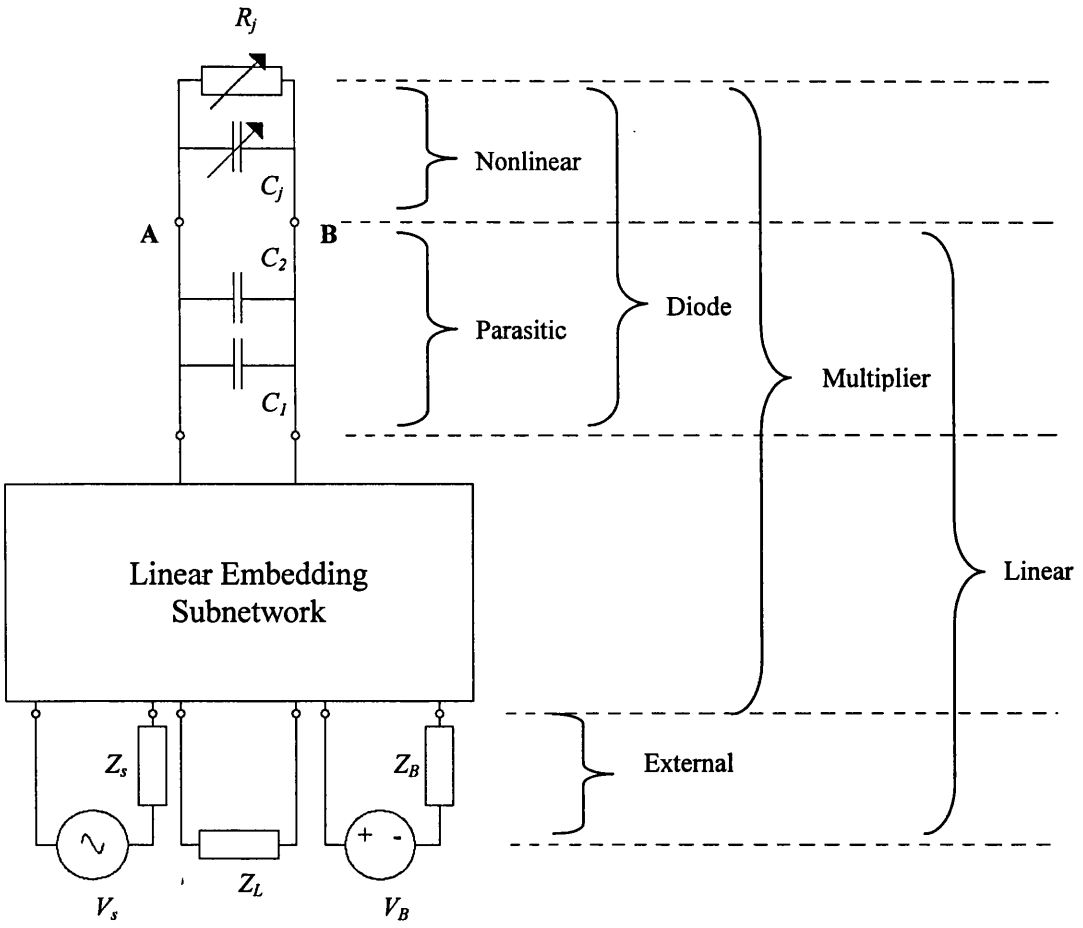


Fig. 6.2 Rearranged circuit schematic of the frequency multiplier indicating linear and nonlinear components. Parasitic components are also included for discussion about the difference between HFSS basic and advanced models. R_j and C_j are the diode nonlinear resistance and capacitance respectively, C_1 and C_2 are parasitic elements of the diode structure, V_B and Z_B are the DC bias voltage and the DC source impedance.

It would be appropriate to indicate here the difference between the HFSS basic and advanced multiplier structures. The basic multiplier structure implemented a gap source bridging two sections of microstrip. No detail of the diode geometry or the layer structure of the GaAs material was included. Embedding impedance values calculated using the basic model could be described by the *Linear Embedding Subnetwork* in Fig. 6.2 but would omit the parasitic elements C_1 and C_2. Values calculated for C_1 and C_2 (see chapter 4) could be added to the embedding impedance but this was not done due to the order in which this work was carried out. This resulted in an incomplete model and consequently gave unrealistically high predications of output power and efficiency. The advanced model was much more realistic in terms of what was included in the HFSS analysis. All possible detail of the diode and the GaAs layer structure including the SiO_2 insulating layers were

included in the advanced model. This encapsulated more of the parasitic components of the diode resulting in a more realistic embedding impedance. This resulted in predictions of output power and efficiency lower than that using the basic model due to the extra reactive losses.

The piecewise technique suggests that the linear and nonlinear subnetworks (see Fig. 6.2) can be split at the point **A-B**, and each subnetwork can be augmented with its own source as shown in Fig. 6.3, which are directly related with each other. The nonlinear circuit can then be analysed using a nonlinear approach and the linear circuit can be solved using a linear transformation. The key to solving the harmonic balance is to find a set of V(t) that give the same current in both subnetworks.

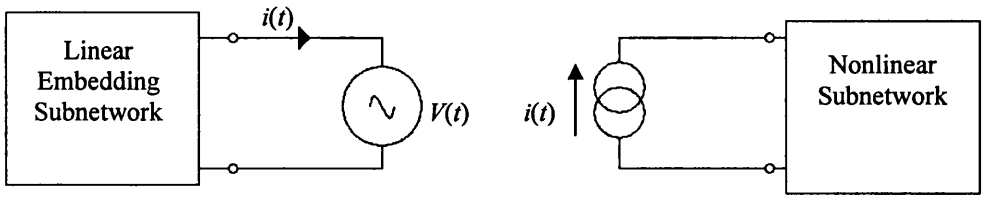


Fig. 6.3 Augmenting individual circuits produced by splitting the circuit in Fig. 6.2 at the point **A-B** with current and voltage sources where $i(t)$ and $V(t)$ are the current and voltage waveforms.

The piecewise technique needs just the frequency domain solutions of the linear subnetwork, i.e. the embedding impedance, of the multiplier to be known in order to derive the harmonic balance equations. Therefore if the multiplier response is to be determined over its operating bandwidth then the embedding impedance is needed at the first and second harmonics and all frequencies encompassed in the bandwidth.

6.2 Multi-Reflection Algorithm

A very useful algorithm was developed by Kerr [6.5] in 1975. The method expands the circuit in Fig. 6.2 lengthening the transmission line at the point **A-B** (assuming the parasitic elements are accounted for in the linear subnetwork) as shown in Fig. 6.4. The long lossless transmission line (of length $l = N\lambda_0$ where N is a positive

integer and λ_0 is the wavelength) has been added in such a way that the steady state solution in both circuits is equal. The transmission lines are sufficiently long so that the networks can be solved individually as in Fig. 6.3.

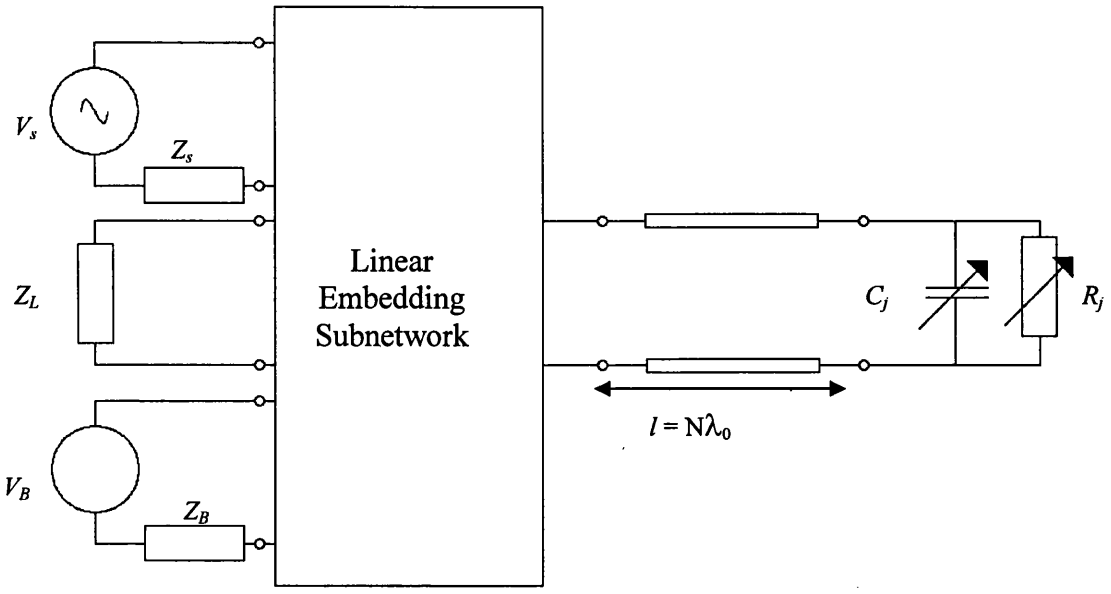


Fig. 6.4 The linear and nonlinear subnetworks are separated by a length of transmission line an integer number of wavelengths long.

A voltage waveform generated in the source propagates to, and is incident upon the diode. Reflections of this signal occur at the diode calculated from the nonlinear time domain analysis. The reflected signal travels back to the linear network where more reflections occur and are, effectively, added to the originally transmitted waveform. Reflections occur again at the diode and the process is repeated until a steady state solution is found. The steady state solution will be indicated by a minimal variation in the incident wave between iterations.

6.3 Harmonic Code Modifications

The original harmonic balance code used herein was written by Siegel, Kerr and Hwang [6.1] intended as a program to determine RF mixer performance. A part of this code calculated the large signal voltage and current waveforms across the diode for a set of embedding impedances at the LO and harmonic frequencies. The program then initiated the small signal analysis, which replicated the interaction of the lower power RF signal from, for example, a telescope.

The large signal analysis could be used to determine the power generated in a single diode at the higher harmonics. The program was initially written for whisker contacted diodes and a subroutine was added to override these expressions for the newer planar devices. Parameters such as the anode size, epilayer thickness and n^+ doping density were included as variables to be used as tuning elements in the program.

In addition the original program only determined output power and efficiency for a single input power and reverse bias level. DO loops were added so the program would scan the input power and bias level as these were the major external tuning capabilities that could be performed in practice.

6.4 Harmonic Balance Analysis Results

This section gives the results of the harmonic balance analysis for the basic and advanced multiplier structures. In each case the HFSS model was used to determine the embedding impedance at the fundamental and second harmonic. Unless otherwise stated the results recorded have been tuned in input power and bias to give the best performance. The input power range was up to 250 mW and the bias was taken between -2 and -18 V.

6.4.1 Basic Multiplier Structure

The basic multiplier structure used is described in the first sections of Chapter 5 and is pictured in Fig. 6.5. The model does not include structural details constituting the parasitic elements of the diode. Results in this section are therefore overestimated in terms of predicted output power and efficiency.

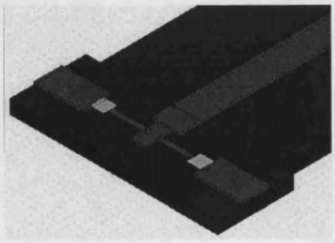


Fig. 6.5 Showing the basic multiplier structure used in HFSS.

6.4.1.1 Optimizing L_{eff}

The initial step used to optimize the multiplier structure was to consider the embedding impedance as a function of effective backshort position, L_{eff}. The embedding impedance of the basic structure as a function of L_{eff} is shown in Fig. 6.6. It was expected that the optimum effective backshort position will be where the embedding impedance has a low real and a high positive imaginary component. This is reflected in Fig. 6.7 which shows the multiplier output power and efficiency as a function of L_{eff}, (all results given herein are for a fixed input power of 250 mW). The optimum value of L_{eff} was found to be 1.07 mm.

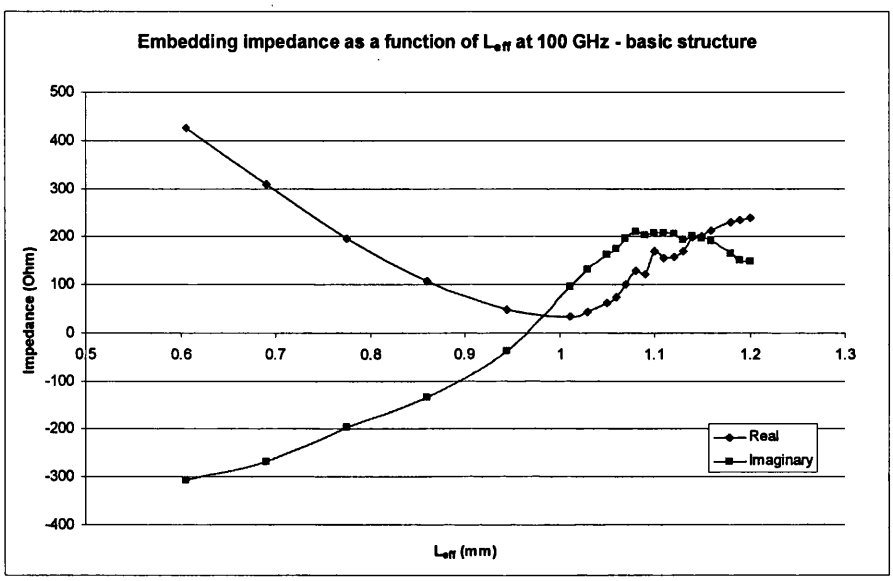


Fig. 6.6 Graph showing embedding impedance as a function of effective backshort position L_{eff} for the basic multiplier structure at 100 GHz.

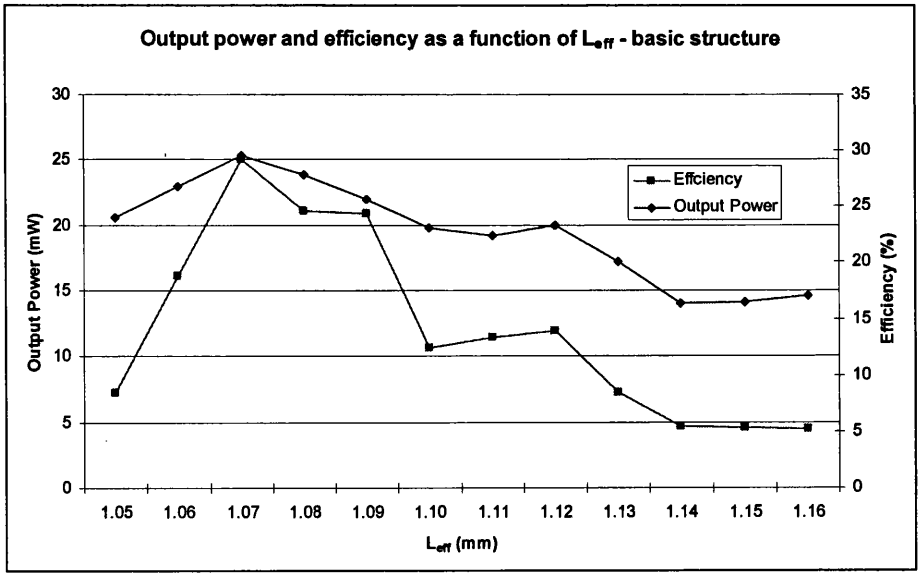


Fig. 6.7 Graph showing output power and efficiency as a function of L_{eff}.

6.4.1.2 Optimizing Anode Diameter

The size of the anode diameter will directly affect the zero bias level capacitance of the diode and can be varied in the multiplier code. If the anode area is too small, current saturation can occur at low drive levels resulting in inefficient multiplying as described in Chapter 4. If the area is too large the extra capacitance will simply act as a lossy component in the multiplier circuit. This being true, the multiplier could, in theory, be optimised to work with any size of anode provided a good match could be found. Fig. 6.8 graphs output power and efficiency as a function of anode diameter for the basic multiplier structure.

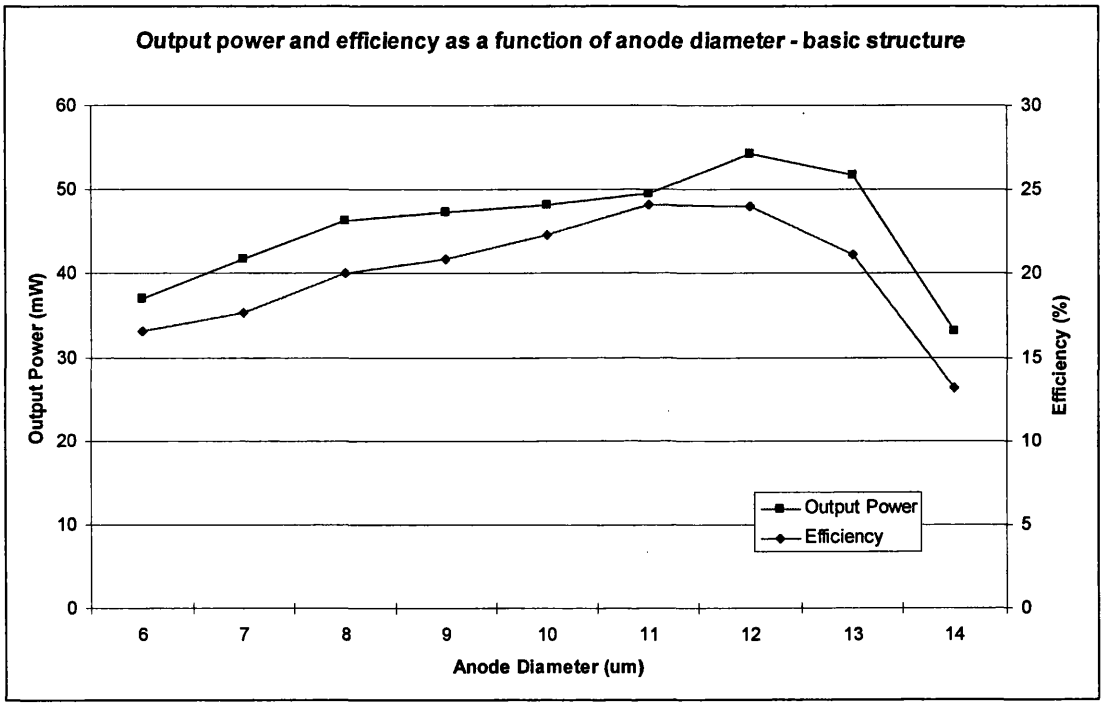


Fig. 6.8 Showing output power and efficiency as a function of anode diameter.

6.4.1.3 Optimizing Epilayer Doping Concentration

The depletion region capacitance is directly proportional to the epilayer doping concentration, N_D, and increasing its value will increase the junction capacitance. Conversely, lowering the doping level of the epilayer will increase the undepleted epilayer impedance and hence the overall series resistance of the diode. The saturation current through the diode is also directly related to N_D where higher doping levels will give higher attainable currents. There will obviously be a trade-off between these variables giving the best performance. The output power and efficiency as a function of N_D is shown in Fig. 6.9.

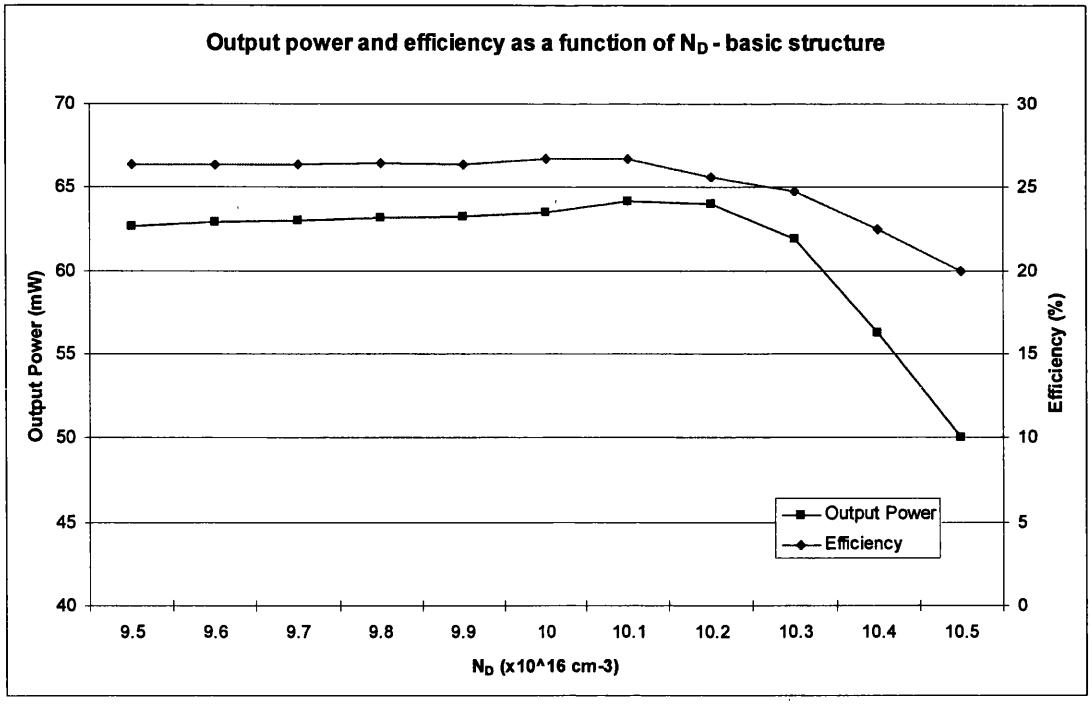


Fig. 6.9 Output power and efficiency as a function of epilayer doping concentration N_D.

6.4.1.4 Output Power and Efficiency – Basic Structure

With L_{eff}, N_D and the anode diameter set to give the best possible results, the frequency response of the basic structure could be determined. The simulated results for the multiplier output power and conversion loss as a function of output frequency are shown in Fig. 6.10 and Fig. 6.11 respectively. The simulated conversion loss 3 dB bandwidth is roughly 8GHz (at 250 mW input power) which is 4.0 % of the central frequency and 7.5 GHz (at 50 mW input power) which is 3.75 % of the central frequency. The peak output power was 57 mW with an input power of 250 mW and 4.4 mW with an input power of 50 mW. The peak conversion loss was -6.5 dB for 250 mW input power (22 % efficiency) and -10.6 dB for 50 mW input power (8.8 % efficiency). Fig. 6.12 shows the output power and efficiency as a function of input power. This indicates the high drive levels needed to operate the multiplier with minimum conversion loss. The power levels needed to get a conversion loss of -6.5 dB, as indicated on Fig. 6.12, are very high. These high levels would probably cause the diode to fail through overdriving. Other effects not accounted for in the harmonic code, such as the thermal properties of the diode, would also alter the appearance of this graph. The higher drive levels would produce higher currents in the diode and therefore higher operating temperatures. This would result in an increase in the diodes resistance and a subsequent drop in efficiency.

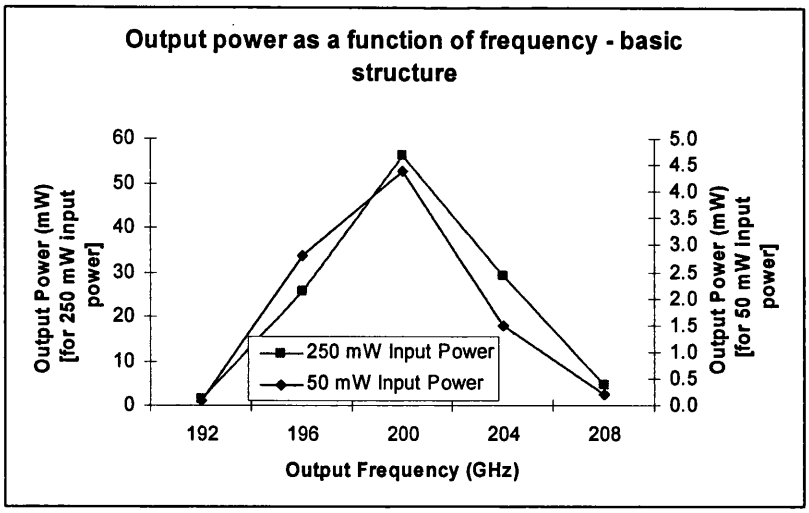


Fig. 6.10 Showing output power as a function of output frequency.

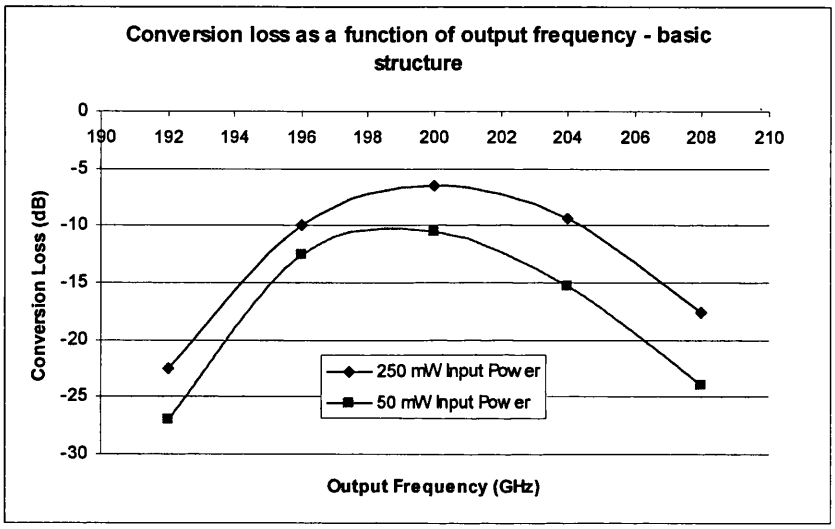


Fig. 6.11 Multiplier conversion loss as a function of output frequency.

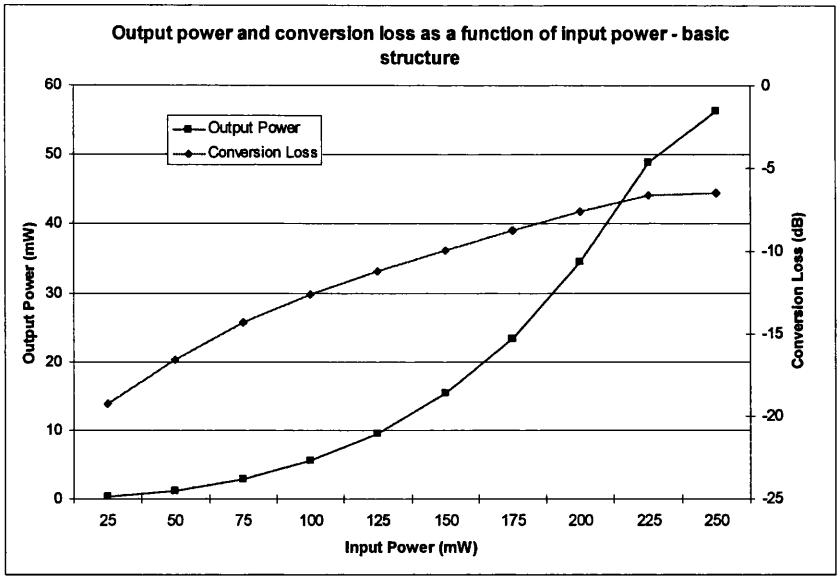


Fig. 6.12 Output power and conversion loss as a function of input power at 200 GHz.

6.4.1.5 Diode Series Resistance

A large effort was made during fabrication to reduce the diode series resistance, R_s. A higher series resistance results in more power dissipated in parts of the circuit that cannot produce higher order harmonics. This essentially means there is less power to generate the output frequencies when R_s is high. This effect is clearly demonstrated in Fig. 6.13 which shows output power and efficiency as a function of diode series resistance. The graph shows that an increase in resistance from 5 Ω to 15 Ω will result in a drop in efficiency of over 12% for an input power of 250 mW at 200 GHz output frequency.

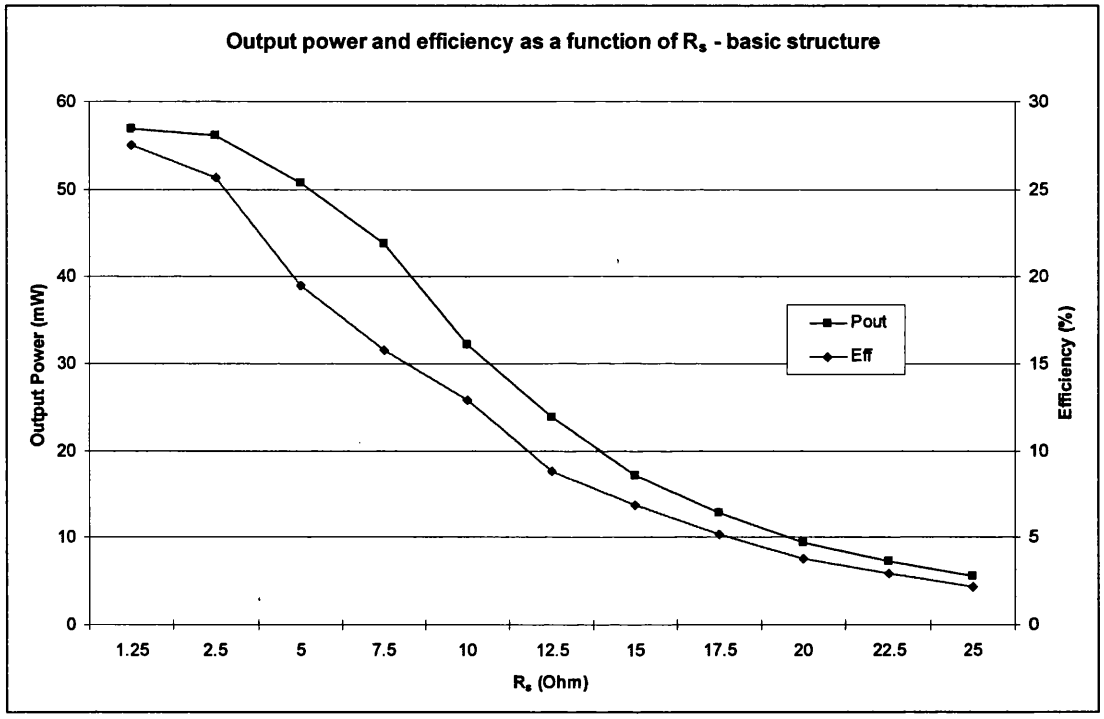


Fig. 6.13 Output power and efficiency as a function of diode series resistance at 200 GHz and 250 mW input power.

6.4.2 Advanced Multiplier Structure

This section repeats many of the simulations performed above but using the advanced multiplier structure which contained more detail around the diodes shown in Fig. 6.14. The advanced structure gives a more realistic impression of what the embedding impedance of the multiplier will be, including the diode parasitic elements, such as C_1 and C_2 in Fig. 6.2, neglected from the basic model.

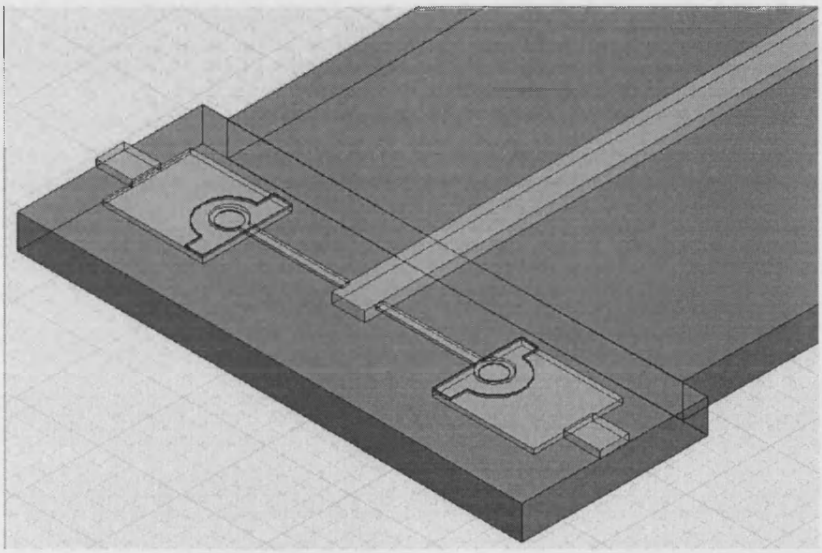


Fig. 6.14 Showing the added detail of the advanced structure compared to that of the basic model in Fig. 6.5.

6.4.2.1 Optimizing L_{eff}

Modifications to the multiplier structure resulted in a dramatic change in the embedding impedance and a sweep in L_{eff} was performed to re-evaluate the optimum effective backshort position. A broad sweep in L_{eff} between 0.85 – 1.07 mm was initially performed to determine the most likely optimum position. The embedding impedance as a function of this sweep is shown in Fig. 6.15. By looking back to Fig. 6.6 the difference in the embedding impedance is apparent. The peak in the imaginary component is much lower in the advanced model by about 100 Ω. This results from the parasitic capacitance now being realised in the model and its overall effect was to lower the imaginary components of embedding impedance. The sweep was refined around L_{eff} = 0.85 mm where the multiplier appeared to be operating better than at L_{eff} = 1.07 mm as in the basic structure. The embedding impedance as a function of effective backshort position between L_{eff} = 0.81 mm and 0.89 mm is shown in Fig. 6.16. Using the Z_{emb} data from Fig. 6.16 the output power and

efficiency could be plotted as a function of L_{eff} and the results of this are shown in Fig. 6.17. This gave the new optimum effective backshort position for the advanced structure at 0.85 mm.

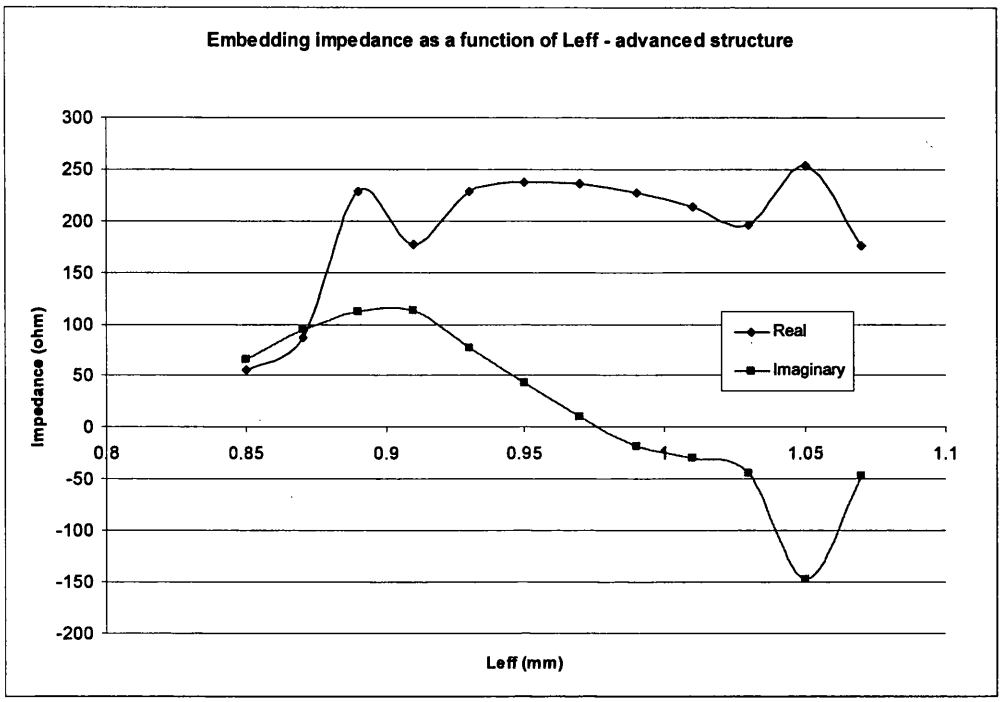


Fig. 6.15 Embedding impedance as a function of L_{eff} for the advanced multiplier structure at 100 GHz.

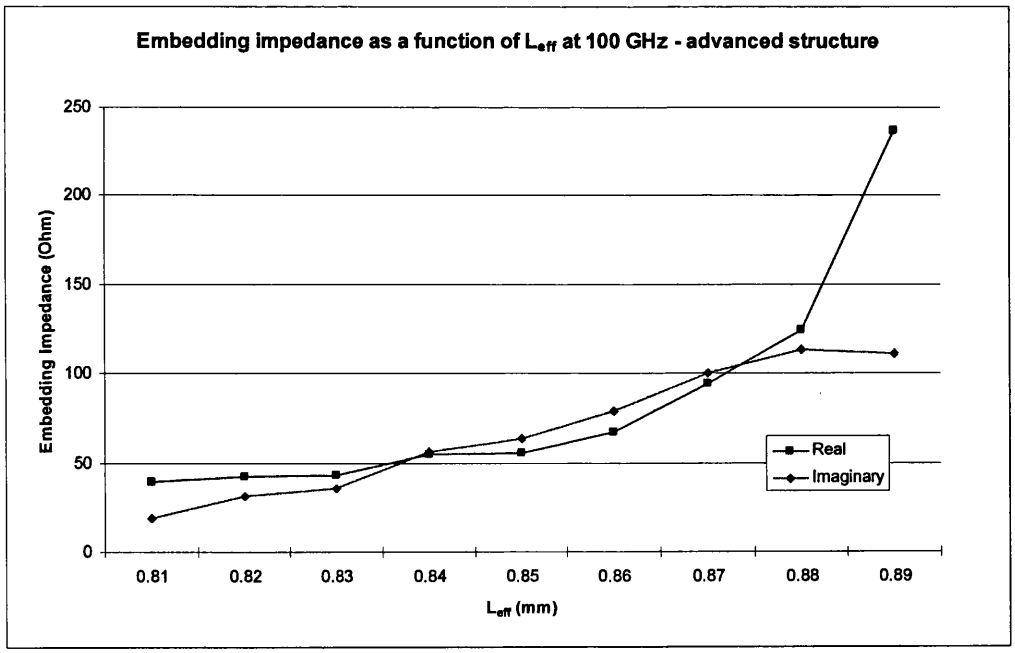


Fig. 6.16 Embedding impedance as a function of L_{eff} at 100 GHz for the advanced structure.

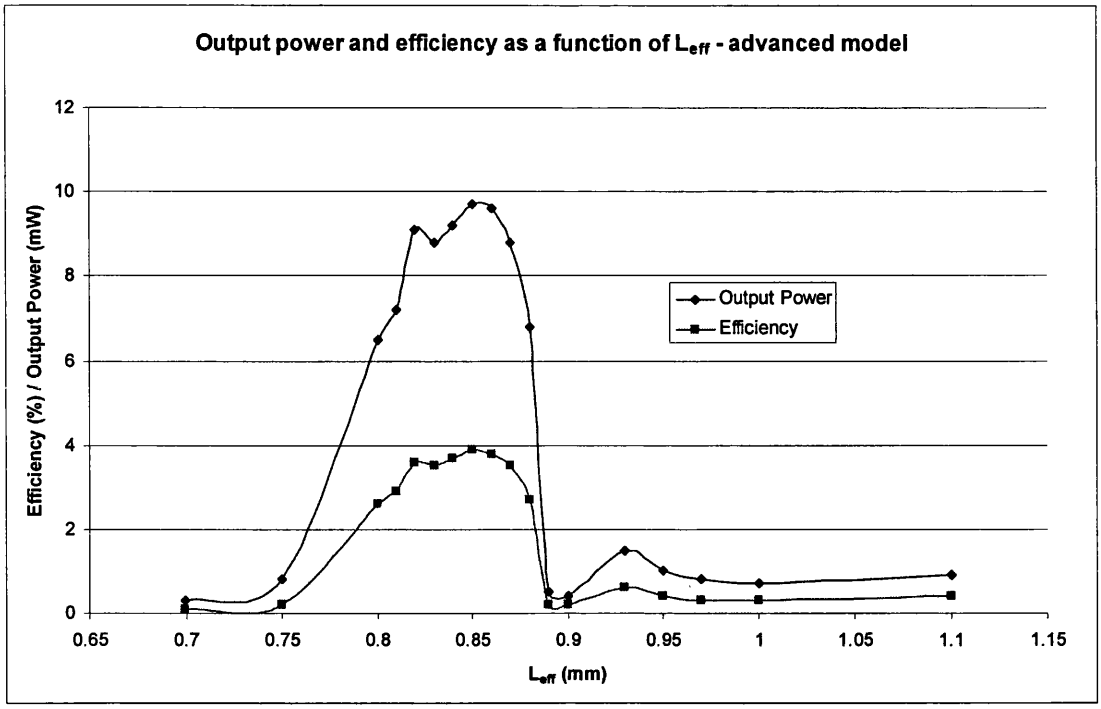


Fig. 6.17 Output power and efficiency as a function of L_{eff} for the advanced structure optimised at 200 GHz and for 250 mW input power.

6.4.2.2 Output Power and Efficiency – Advanced Structure

With the optimum position of the effective backshort determined for the advanced structure, the frequency response of the advanced multiplier structure could be determined. The simulated multiplier output power and efficiency as a function of output frequency are shown in Fig. 6.18 and Fig. 6.19 respectively at L_{eff}= 0.85 mm. Conversion loss for the advanced multiplier structure is shown in Fig. 6.20 suggesting the 3 dB bandwidth is 9.5 GHz (at 250 mW input power) which is over 4.7 % of the central frequency and 7.0 GHz (at 50 mW input power) which is 3.5 % of the central frequency. This figure is approximately equal to that of the basic model but the addition of the parasitic capacitance has obviously severely reduced the overall performance of the multiplier. The peak output power dropped from 52 mW in the basic model to 12 mW in the advanced model at 250 mW input power. With an input power of 50 mW the output power was just 0.7 mW in the advanced model. The peak efficiency in the advanced model with an input power of 250 mW was 4.6 % which corresponds to a peak conversion efficiency of -13.2 dB at 198 GHz. With 50 mW input power the peak efficiency is just 1.4 % which corresponds to a conversion efficiency of -18.6 dB at 198 GHz.

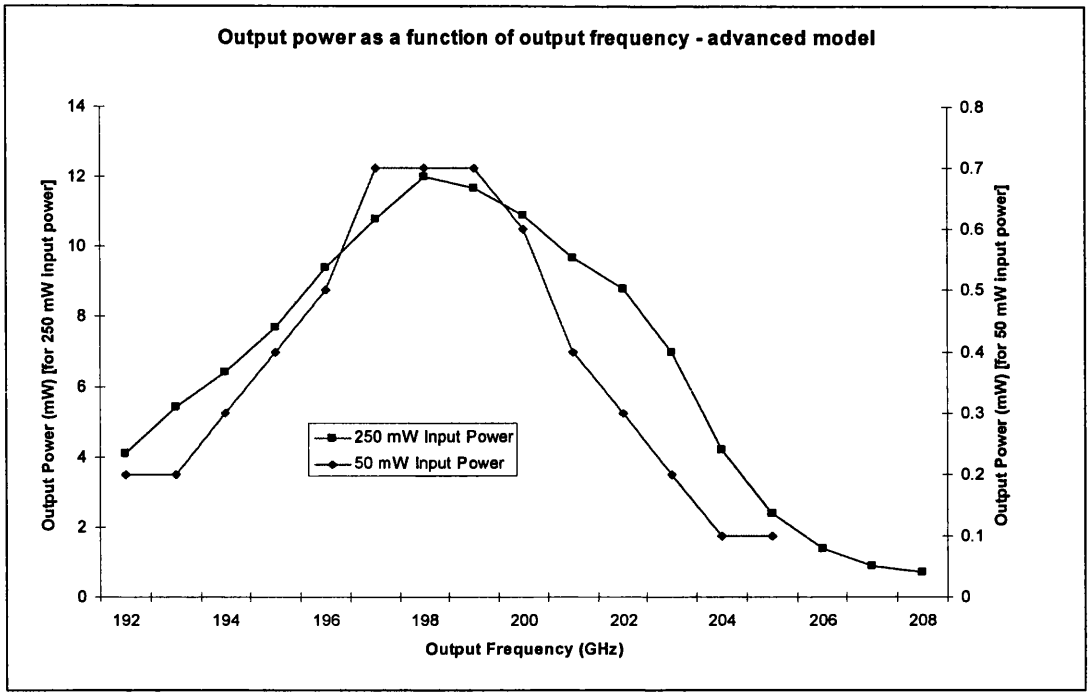


Fig. 6.18 Output power as a function of output frequency for the advanced multiplier structure at L_{eff}= 0.85 mm.

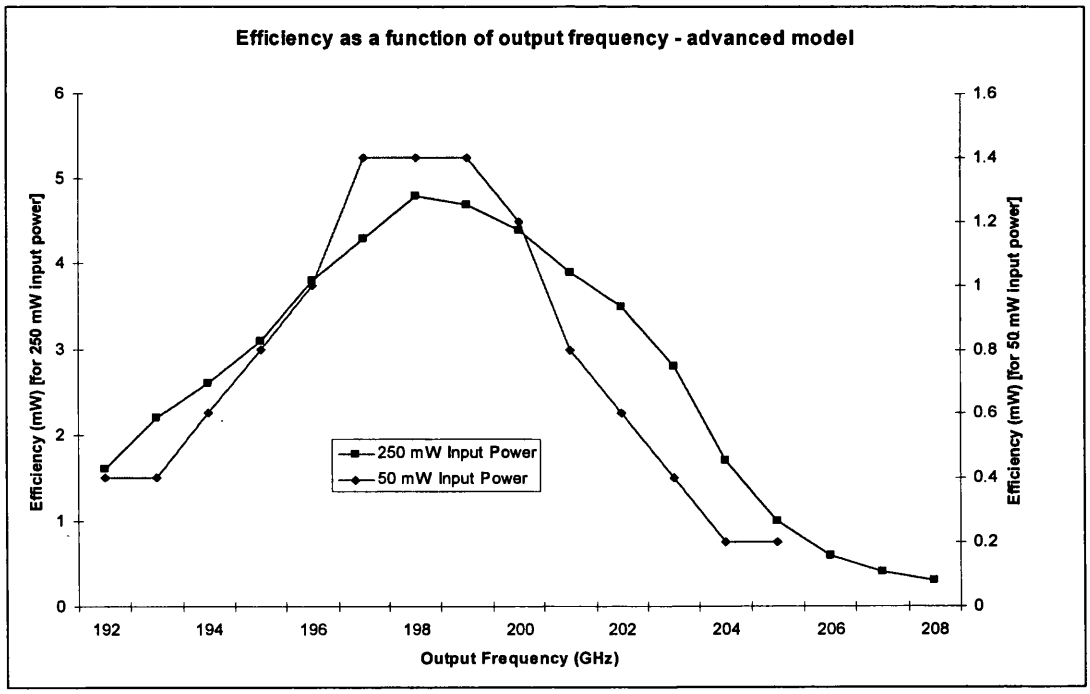


Fig. 6.19 Efficiency as a function of output frequency for the advanced multiplier structure at L_{eff} = 0.85 mm.

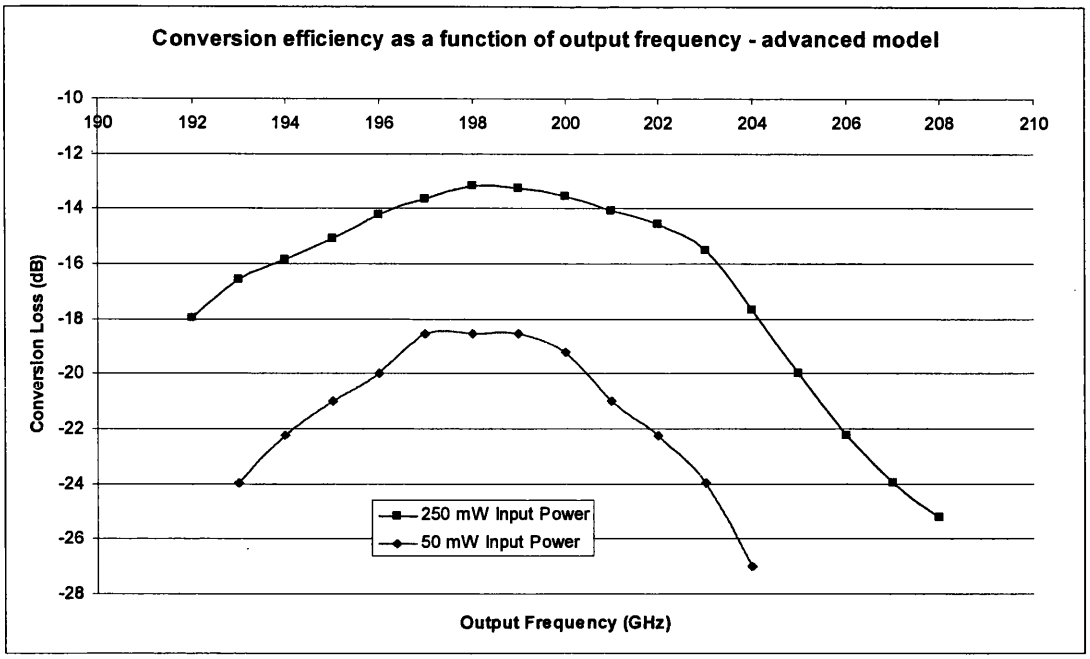


Fig. 6.20 Conversion loss as a function of output frequency for the advanced multiplier structure

References – Chapter 6

[6.1] P. Siegel, A. Kerr, W. Hwang, "Topics in the optimization of millimeter waves mixers," *NASA Technical Paper 2287*, 1984.

[6.2] M. S. Nakhla, J. Vlach, "A piecewise harmonic balance technique for determination of periodic response of nonlinear systems," *IEEE Transactions on Circuits and Systems*, vol. cas-23, no. 2, February 1976, pp. 85-91.

[6.3] E. M. Baily, "Steady state harmonic analysis of nonlinear networks," Ph.D. dissertation, Stanford University, Stanford, CA, 1968.

[6.4] J. C. Lindenlaub, "An approach for finding the sinusoidal steady state response on nonlinear systems," *Proceedings of the 7th Annual Allerton Conference on Circuit and Systems Theory*, University of Illinois, Chicago, 1969.

[6.5] A. R. Kerr, "A technique for determining the local oscillator waveforms in a microwave mixer," *IEEE Transactions on Microwave Theory and Techniques*, October 1975, pp. 828-831.

Chapter 7

Multiplier Fabrication

This chapter covers all the fabrication aspects of the multiplier circuit carried out in the David Bullet Nanofabrication Laboratory and the Terahertz Technology Laboratory at the University of Bath. Semiconductor processing techniques are described covering all methods used in the final construction. Producing reliable working Schottky diodes with a low ideality factor, η, and low series resistance, R_s, was one of the critical obstacles faced. As mentioned in Chapter 6 small increments in R_s can produce sharp increases in multiplier conversion loss and a large effort was made to minimise R_s in the production of the diodes.

Producing the thin (20-50 μm) membrane substrate also required considerable attention. Many methods were implemented with success found in a combination of dry etching and wafer lapping. Warping, surface roughness and device under-etching were all issues during the membrane processing.

The multiplier block was made using a CNC mill which was programmed using simple g code in a DOS based PC application. Issues arose with the alignment of the bottom and top halves of the multiplier split block. Refined programming code in appreciation of minor backlash compensation sufficiently resolved these issues. Mounting and electrical contacting of the multiplier chip into the block were the final steps in the fabrication.

7.1 Introduction to Semiconductor Processing

7.1.1 Cleaning Procedures and Preparation

In all semiconductor processing it is essential to ensure the wafer surface and working environment are as clean as possible. Impurities on a wafer surface can lead to defect devices and lower yields. This is more important from an industry stand point than from a research one. However, this research had budget and time restrictions and it was important to minimise unusable devices.

7.1.2 Photomask Design

The photomask was designed using a standard CAD software package. Fig. 7.1 represents a small area of the mask showing some test diode patterns, alignment marks, the multiplier diodes and microstrip transmission line and part of the first element of the RF filter. The mask had to accommodate several key features which were considered during the design. The mask cell was chosen to be 10 x 10 mm so that up to 16 cells could fit onto a single mask and to reduce the amount of expensive GaAs material that was used in each batch (typically a 11 x 11 mm GaAs chip could be used). Of most importance was the ability to adjust L_{eff}, the effective backshort position, by a known amount during the patterning of the wafer to give the design greater flexibility. This was done so that any further refinement of the multiplier design involving changing L_{eff}, and hence mask design, would not invalidate the mask. This was achieved by patterning the transmission lines and filter on separate cells that could overlap and the relative offset measured on a sliding scale, see Fig. 7.1. This also allowed two other variations to be implemented in the mask design; variation in anode diameter and a 4-diode multiplier. Both of these variations would also require a tuning of the circuit which could mostly be achieved by varying L_{eff}. These extra features were introduced in the understanding that their use would be supplementary to this project, and included for possible future research.

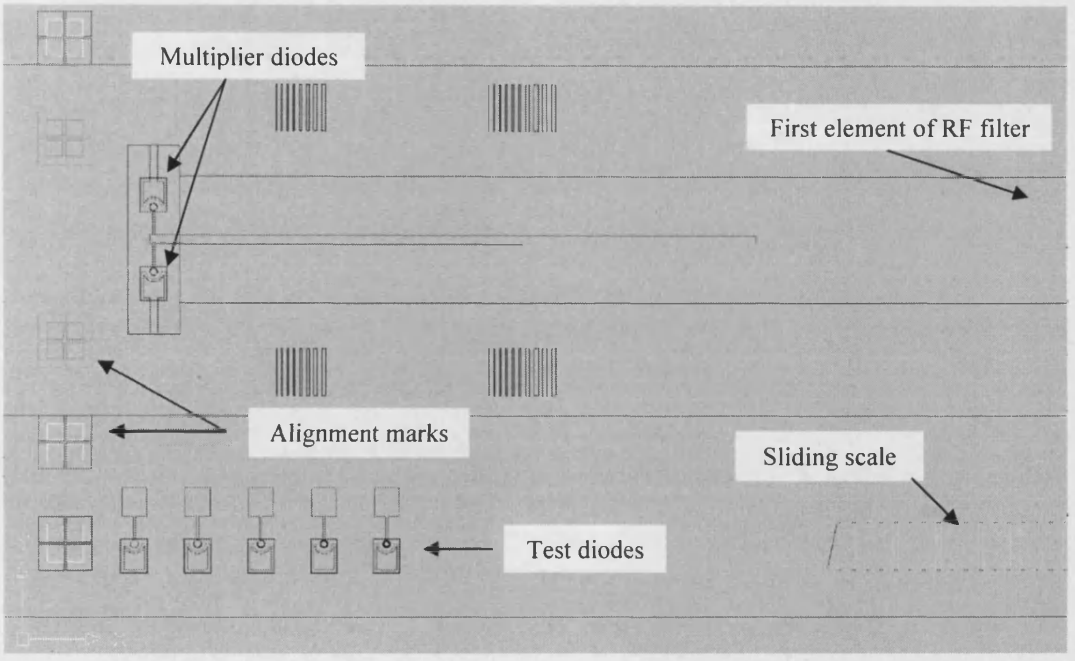


Fig. 7.1 Outline of a small area of the mask showing various features.

Alignment marks were patterned onto the wafer chip in the first stage of lithography and overlay registration was used to align to the subsequent cells. Additional alignment marks were included in the ohmic contact stage of patterning for increased accuracy of positioning between anode and ohmic contact. In retrospect all alignment marks should have been deposited in the ohmic contact stage to save time and improve accuracy. The lithography stages were: 1) alignment marks, 2) ohmic contacts, 3) anodes, 4) anode fingers and transmission lines, 5) filter patterns, 6) diode protection for dry etching, 7) deep multiplier outline etch.

Stages 2 and 3 are critical for good working Schottky diodes and form nearly half of the work in processing. Stages 6 and 7 form the other half of the processing work, the production of good dry etched GaAs profiles for the multiplier.

7.1.3 Photolithography and E-Beam Lithography

Most of the patterning in this project was done using contact photolithography. Patterns are created by exposing a photosensitive resist (coated on the surface of the wafer chip) through a photomask using a strong UV light source. Positive resists were used throughout the processing where the exposed areas are removed in the subsequent development stage. Development is in a sodium hydroxide based solution, Microposit 351, and is diluted 3.5:1 in de-ionised (DI) water. The resists used were Shipley 1813 (for thicknesses ~1.5 μm) and Microposit 220-7.0 (for thicknesses between 5 and 9 μm). The thick resists were used for deep dry etches and thick metal layers > 1000 nm. Contact photolithography is quick and relatively easy and with the correct resist thickness, patterns down to 1 μm can be obtained. Problems can arise due to the contact between mask and wafer such as cracking or lifting of the resist.

E-beam lithography was used in the early stages of this work as the patterns can be created in a CAD environment and do not have to be committed to a photomask. High energy electrons are used to directly write onto the wafer chip surface which is coated in a resist sensitive to the e-beam. An accurate stage under computer control is used to move the semiconductor chip in relation to the beam which writes the

pattern. E-beam lithography is used for patterning sub-micron features and in some cases the beam spot size can be focussed down to < 10nm.

7.1.4 Wet and Dry (RIE) Etching

Wet and dry etching formed an essential part of the processing for the multiplier devices. Wet chemical etching of GaAs was needed to form the surface recess required to deposit the ohmic contact into. A typical GaAs wet etch solution would consist of a mixture of sulphuric acid, hydrogen peroxide and DI water [7.1]. Hydrofluoric acid was needed to wet etch silicon dioxide during various stages of the processing [7.2]. Removing unwanted n and n^+ GaAs material, providing device isolation, and forming the multiplier chip outline, so that each circuit could be separated from the substrate, was achieved using Reactive Ion Etching (RIE), a form of dry etching. RIE uses plasma enhanced chemical reactions to remove material and can be used to produce highly anisotropic etch profiles using standard resist patterning. Typical gases used during dry etching were chlorine (Cl_2), silicon tetrachloride ($SiCl_4$) and argon (Ar_2) [7.3]. All RIE was performed in a Plasmalab 80 built by Oxford Instruments.

7.1.5 Material Deposition and Coating

Material deposited onto a substrate was done using either an Edwards 306 thermal evaporator or an Edwards E-Beam evaporator. By passing the correct high voltage through a tungsten boat the material to be deposited (situated in the boat) reaches melting point and starts to evaporate upwards in the vacuum chamber. Adjusting the voltage across the boat will determine the rate at which material is deposited on the sample surface and this is monitored using a piezoelectric crystal. The wafer samples are mounted upside-down in the vacuum chamber so that the evaporated material adheres to the sample surface. The e-beam evaporator operates by firing a targeted beam of electrons at a sample of metal inside a crucible of high melting point. The beam current is adjusted to initiate the metal evaporation and the deposition rate of the metal. Ohmic contacts were made in the thermal evaporator and all other metal deposition was predominantly done in the e-beam evaporator.

It was also necessary to deposit SiO_2 during the course of this work which was achieved using Plasma Enhanced Chemical Vapour Deposition (PECVD). The

plasma enhanced reaction between silane (SiH_4) and a source of oxygen such as N_2O at the correct temperature and pressure can be used to deposit thin layers of SiO_2 [7.4, 7.5].

An Ultra High Vacuum (UHV) system was used to sputter tungsten as an anode material, [7.6]. High energy argon ions bombard a tungsten cathode as they are accelerated in a large potential gradient. Tungsten atoms near the surface are vaporised through momentum transfer and deposited on the GaAs substrate as a thin film. The tungsten atoms that arrive at the substrate surface are also highly energetic and can damage the semiconductor surface. This can be rectified by annealing the sample at 400K for 2-4 minutes to unify the metal on the surface [7.7].

Electroplating is also a technique for depositing metals. An electrolytic platinum solution was used on a heated probing station where a pulsed current could be delivered to the solution coating the sample [7.8, 7.9].

7.1.6 Wafer Lapping

In order to separate each multiplier circuit a mechanical lapping method was implemented after all front-side processing. Wafer samples were mounted face down on a glass block using a robust wax, solid at room temp and easily applicable at 150°C. The lapping was performed using a Logitech PM5 grinding/ polishing jig and grinding was performed on a glass plate using an alumina solution seeded with 3 μm particles.

7.1.7 Wafer Profiling

It was essential to accurately know the surface profile of the wafer chip during processing. This is especially important after wet and dry etching or after patterning resists for dry etch masking. Etch depth profiles were required to understand etch rates and similarly resist heights needed to be measured to determine selectivity during dry etching. A Dektak surface profiler was used for this purpose that could accurately measure down to 100 nm. The Dektak utilises microactuators to respond to the vertical movement a fine diamond tipped needle that is driven across the wafer surface resulting in minor voltage fluctuations. The voltage is calibrated into a distance and the results are plotted as a cartesian graph on screen.

7.1.8 Gallium Arsenide Processing Overview

Fig. 7.2 shows the semiconductor processing steps that are described below. The two most important sections; the Schottky contact and membrane fabrication are covered in more detail in subsequent sections. Wafer layer structure used in final device processing was (from bottom up); semi-insulating GaAs substrate, 3 μm highly doped ($1x10^{18}$ cm^{-3}) n^+ GaAs layer, 1 μm low doped ($1x10^{17}$ cm^{-3}) n GaAs layer and capped with a 0.25 μm SiO_2 electrically insulating layer.

Step 1: GaAs wafer is cut into smaller 11x11 mm samples using a diamond scribe. The GaAs wet etch (Step 6) was needed to etch under the fingers of the diodes quicker than towards the diodes themselves. Therefore the diode fingers were aligned perpendicular to the [110] GaAs crystal direction to give the correct undercut profile.

Step 2: The smaller samples were cleaned and coated with resist, then patterned with alignment marks. Then a thin layer of titanium followed by gold was evaporated. The resist was then dissolved in a solvent removing the unwanted deposited metal and leaving the alignment marks. This lift-off procedure was used for all metal evaporations but these details shall be omitted from the following steps.

Step 3: Patterning the ohmic contacts, wet etching SiO_2, wet etching 1.5 μm GaAs and then depositing the ohmic contact material. The ohmic contact was made by alloying germanium and gold. A titanium barrier was used in between the alloy and a thick gold capping layer.

Step 4: Anodes were patterned in Shipley 1813 resist and a HF wet etch of SiO_2 was performed to open the anode holes to the n GaAs surface. The fingers and transmission lines were then patterned and developed using the same resist. Finally the filters were patterned using the sliding scale to adjust L_{eff} accordingly. The anode layers were evaporated and capped with a thick gold layer. This procedure completed three lithography levels in a single step and greatly reduced processing time. Although very quick this technique often resulted in the final resist film being

slightly damaged. This could be alleviated to some extent by leaving the sample to dry sufficiently after each development.

Step 5: Protection patterns of resist were formed over the diode active areas and the sample was dry etched using RIE. The dry etch was performed to remove the *n* and n^+ doped layers using mainly the thick metal deposited in step 4 as a mask. The good selectivity between gold and GaAs meant that the gold only etched fractionally during the 6 μm deep dry etch. The anisotropic behaviour of the $SiCl_4$ based RIE resulted in near vertical side walls and a mirror-like etched surface.

Step 6: This step involved isolating the individual devices without under-etching the Schottky contacts. Adhesion problems at the SiO_2 and *n* GaAs interface were observed during this step. The final process involved opening a small aperture in a blanket layer of resist (protecting exposed side walls) in between the fingers and wet etching until the air channels were formed. This could be by reading a high resistance when probing between two adjacent ohmic contacts (the current path would favour that through the n^+ layer rather than the diodes if air channel had not etched and the read only a few Ohms). The air channels also provided a reduction in the parasitic capacitance as described in section 4.3.3.

Step 7: Microposit 220-7.0 resist was used in the final deep dry etch around the device circuit. The resist was spin coated to a thickness of 5.5 μm which was adequate for such a long etch. The selectivity between the resist and GaAs in the $SiCl_4$ RIE environment was between 10:1 and 20:1 depending on power, gas throughput, argon levels and chamber pressure. The device circuits were etched down 45 μm around the device providing the membrane ready for lapping.

Step 8: With all top-side processing complete the wafer sample was then front-side mounted parallel to a glass carrier using a robust wax. The sample was then lapped down, as described in section 7.1.6, until the device outlines were visible. The individual multiplier circuits are then carefully removed by washing with a solvent such as acetone.

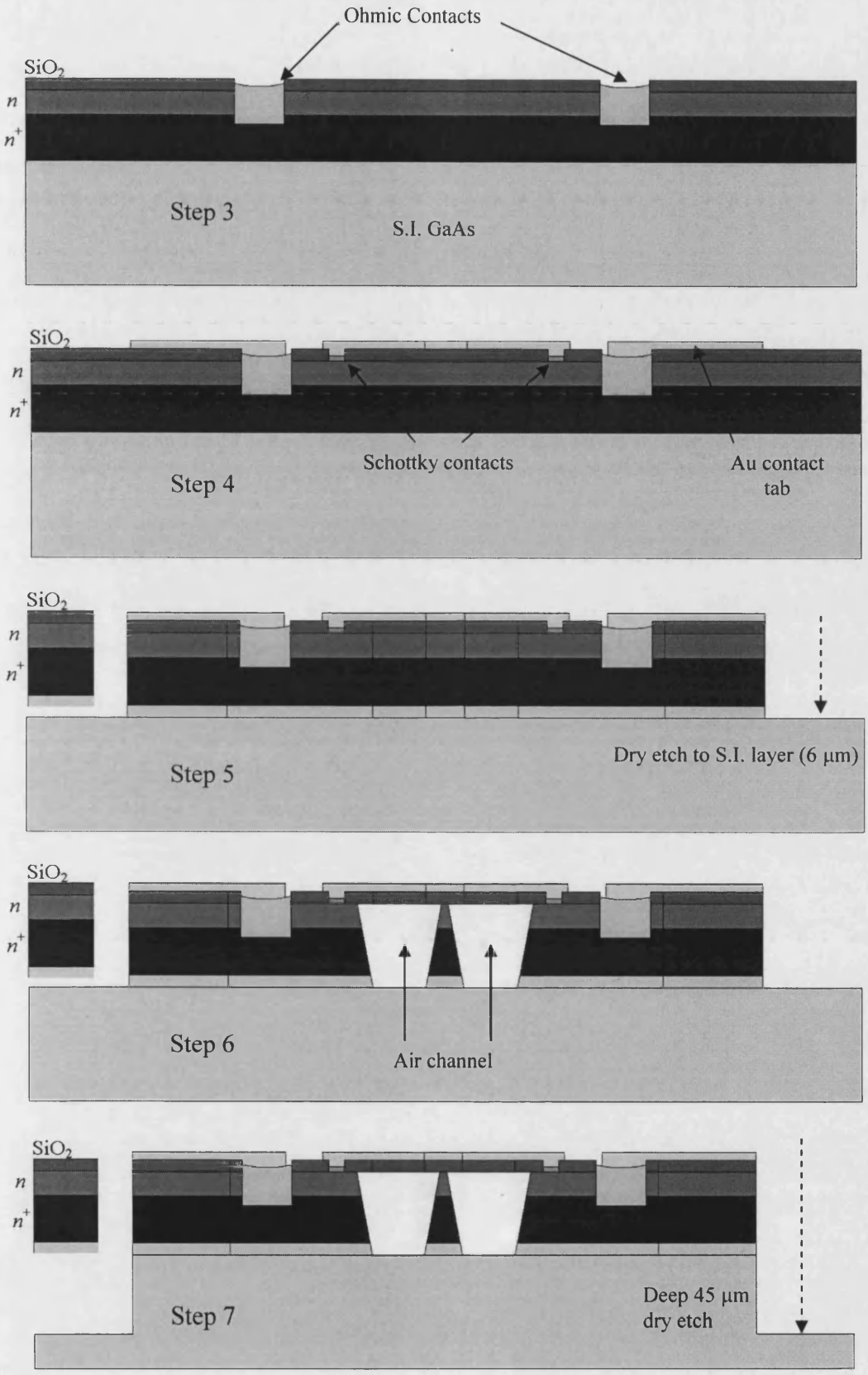


Fig. 7.2 Processing overview of steps 3 to 7 showing the various layers in the GaAs wafer.

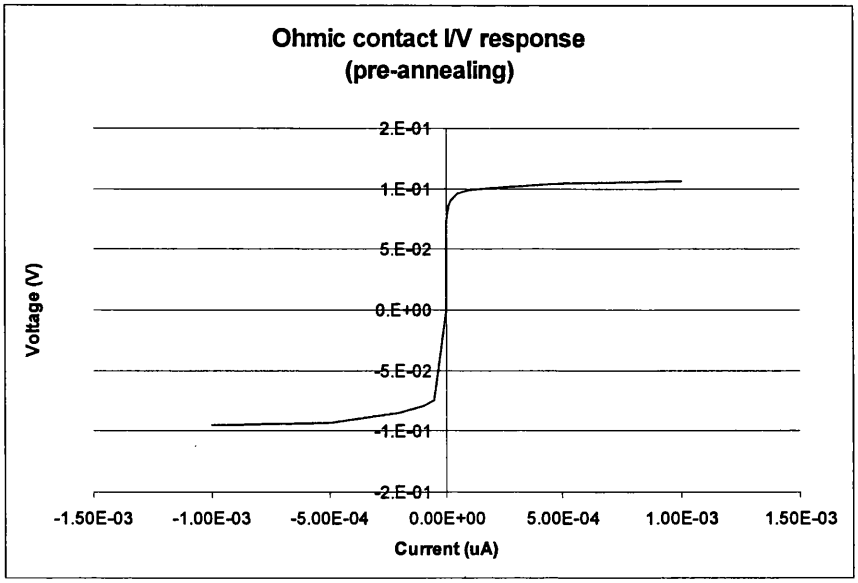
7.2 Schottky Diode Formation

This section will cover the work done in Steps 3 & 4 in section 7.1.8 in more detail. Producing low resistance ohmic contacts was not a major issue in the fabrication but is covered here. The bulk of the work was in developing good Schottky contacts with low variation in characteristics across the entire chip. A low ideality factor, low series resistance and a relatively high reverse breakdown voltage were the key diode characteristics needed for good multiplier performance.

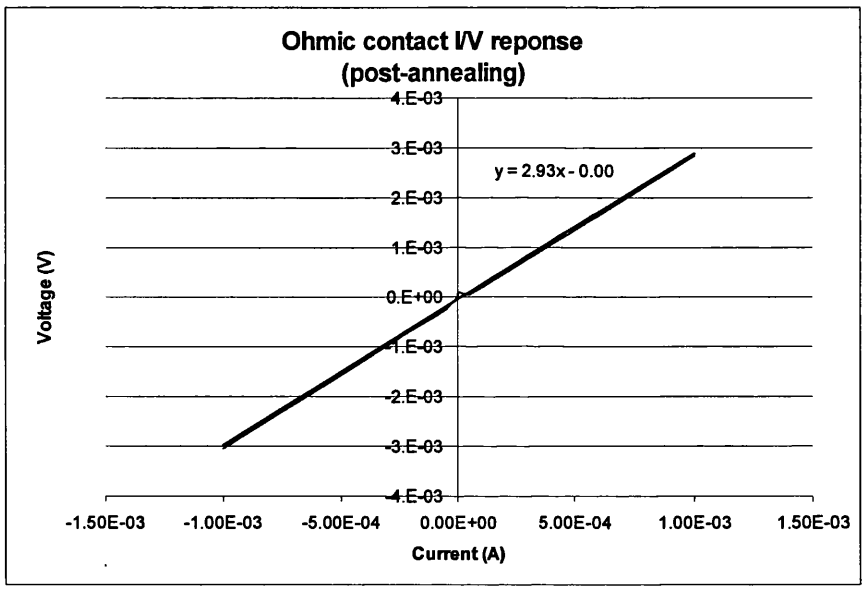
7.2.1 Ohmic Contacts

After etching the GaAs a few hundred nanometres into the n^+ layer a thin layer of germanium and gold was evaporated. A thin layer of titanium is then deposited to act as a barrier for the Ge-Au layer during annealing. This ensures that the Ge-Au layer diffuses into the highly doped n^+ GaAs layer and not into the thick gold layer which is used to cap the contact for good probing or contact to other parts of the circuit.

Annealing the contact is done at a temperature around 450°C in an oxygen free atmosphere. As the temperature rises the gallium diffuses into the gold and some gaseous arsenic is released requiring special filtering of the annealing chamber. The germanium diffuses into the wafer sample, enhanced by the presence of the titanium, and acts as a local dopant near the surface. Gallium then diffuses in to the free sites in the gold produced by the germanium. Fig. 7.3 shows a typical I/V response of an ohmic contact (a) before and (b) after annealing for 2 minutes at 450°C. The ohmic contact resistance shown in Fig. 7.3 (b) (gradient of line = 2.93 Ω) includes the resistance of the metal probes which totals no more than 0.75 Ω. This gives a total ohmic contact contribution of resistance to the diode of ~2.2 Ω. This measurement was taken by probing between two ohmic pads approximately 500 μm apart. All readings of ohmic resistance given herein were taken using this method.



(a)



(b)

Fig. 7.3 Showing the I/V response of an ohmic contact (a) before annealing and (b) after annealing displaying the straight line equation where the gradient is equal to the ohmic resistance equal to 2.93 Ω.

7.2.2 Anode Formation and DC Characteristics

The following sections are sub-sectioned into the different methods of anode formation. Every batch of diodes made has been given a batch name for ease of reference in the text. The batch name follows the syntax UBD-(number). Some of the fabrication procedure has been tabulated for ease of comparison between diode batches. The fabrication and results tables include the following abbreviations:

- Dehy. – sample is dehydrated on a hot plate at 180°C for 15 minutes.
- Resist – Either 'S' for standard Shipley 1813 or 'T' for Microposit 220-7.0 thick resist.
- GaAs Etch – A GaAs wet etch was performed using a sulphuric acid and hydrogen peroxide based etch $H_2SO_4 : H_2O_2 : H_2O$ in the ratio 1:8:1000.
- Oxide Etch – The oxide layer that quickly forms on the *n* GaAs surface when exposed to air was removed using a $HCl:H_20$ etch in the ratio 1:1, the table indicates the time of the etch.
- $(NH_4)_2S$ – Ammonium sulphide was used to prevent surface oxide reforming after surface oxide etch.
- t_m – indicate the thickness of metal that was deposited in nm.
- X – indicates the associated action in the table was not performed.

7.2.2.1 Evaporated Gold Anodes (UBD-1)

Preliminary work on anode formation was done using e-beam lithography to pattern an array of anode sizes ranging in diameter from 1-20 μm. Ohmic contacts were formed in rectangular structures around the edge of the patterns. Anodes were formed by evaporating 10 nm of titanium and 200 nm of gold on the *n* GaAs surface. The *n* GaAs surface had previously been treated with HCl to remove any GaAs oxide.

7.2.2.2 Evaporated Silver Anodes (UBD-2)

Using standard lithography anode sizes 1–20 μm were evaporated using silver as the anode material. A short GaAs oxide etch was performed prior to evaporation. Silver was evaporated directly on the *n* GaAs surface to a thickness of 180 nm.

7.2.2.3 Electroplated Platinum Anodes (UBD-3)

Electroplating platinum anodes was a difficult process with poor yield. Platinum was deposited to a thickness of 180 nm and a GaAs oxide etch was performed prior to this. The results reported were not common to this process. Low yields and inconsistency across the chip sample resulted in this being an expensive and time consuming approach to making anodes. Furthermore, when I/V characteristics were taken the diodes displayed degrading performance over time. However when the correct parameters of substrate temperature, current density and electroplating time

were found, anodes produced using this method showed excellent ideality and series resistance. In light of the problems with this procedure other techniques were implemented for anode formation.

7.2.2.4 Sputtered Tungsten Anodes (UBD-4)

Using standard lithography anode vias were patterned and tungsten was sputtered forming the contacts. The high energy of the sputtered tungsten a damaged the surface of the GaAs which was partly rectified by annealing the sample. Sputtering power was 5-6 mW done in on/off periods of 10 minutes for a total sputtering time of 30 minutes (to allow sputtering head to cool down). A total of 60 nm of tungsten was deposited. A huge improvement in diode ideality could be seen after the tungsten anodes were annealed. This is due to recombination of the damaged surface during annealing. Low ideality and superior stability during I/V testing made this method a strong competitor to the evaporated Ti and Pt anodes.

Batch: UBD-1			**Batch: UBD-2**			**Batch: UBD-3**			**Batch: UBD-4**		
A_r	η	R_s	A_r	η	R_s	A_r	η	R_s	A_r	η	R_s
20	1.15	22.8	20	1.54	14.6	20	1.14	5.6	20	1.09	11.2
19	1.36	13.9	19	1.51	12.2	19	1.12	5.6	18	1.09	87.5
18	1.18	21.4	18	1.70	9.0	18	1.12	5.6	15	1.09	12.3
17	1.28	16.5	17	1.41	21.3	17	1.12	6.7	15	1.16	87.8
16	1.24	20.3	16	1.24	18.0	13	1.11	4.5	14	1.08	20.2
15	1.23	23.2	15	1.36	15.7	12	1.12	5.6	13	1.14	20.2
14	1.25	18.1	14	1.31	20.2	11	1.11	9.0	13	1.10	38.2
R_{oc}		3.4	R_{oc}		~3	R_{oc}		~3	R_{oc}		~3
V_{br}		8.5	V_{br}		8.5	V_{br}		-	V_{br}		~12

Table 7.1 Average DC diode characteristics for batches UBD-1 to UBD-4.

The key DC diode characteristics for UBD-1 to UBD-4 are shown in Table 7.1 where A_r is the diode anode diameter in microns, η is the ideality factor, R_s is the series resistance in ohms, R_{oc} is the ohmic contact resistance in ohms and V_{br} is the diode reverse breakdown voltage in volts.

7.2.2.5 Evaporated Refractory Metal Anodes (UBD-5 to 15)

The refractory metals platinum and titanium were used in the bulk of research into evaporated anodes. Anodes formed with these metals gave stable DC characteristics and high yields usually with good uniformity across the GaAs sample. Samples with evaporated anodes did not need to leave the clean room between lithography and anode deposition (unlike sputtering or electroplating although these could be performed in a clean room if available), an obvious advantage when considering surface oxide formation and contamination. Table 7.2 gives an overview of the key processing elements used during the anode formation.

Batch	Dehy.	Resist	GaAs Etch	Oxide Etch	$(NH_4)_2S$	Metals evaporated t_m (nm)		
UBD-5	•	*S*	X	1 min	X	Pt (35)	Ti (60)	Au (80)
UBD-6	•	*S*	1 min	1 min	X	Ti (50)	Pt (60)	Au (80)
UBD-7	•	*S*	1 min	1 min	1 min	Pt (50)	Ti (80)	Au (60)
UBD-8	•	*S*	30 s	2 min	1 min	Pt (50)	Ti (80)	Au (160)
UBD-9	•	*S*	X	1 min	X	Ti (100)	Pt (20)	Au (150)
UBD-10	•	*S*	X	1 min	X	Ti (60)	Pt (20)	Au (100)
UBD-11	•	*S*	X	1 min	X	Ti (60)	Pt (40)	Au (150)
UBD-12	•	*S*	X	1 min	X	Ti (60)	Pt (40)	Au (200)
UBD-13	X	*T*	X	1 min	X	Ti (60)	Pt (25)	Au (800)
UBD-14	X	*T*	X	1 min	X	Ti (90)	Pt (20)	Au (900)
UBD-15	X	*T*	X	1 min	X	Ti (60)	Pt (40)	Au (940)

Table 7.2 Key processing elements to each diode batch with refractory metal anodes.

Hexamethyldisilizane (HMDS) adhesion promoter was used in all diodes included in Table 7.2. In all cases the time between drying the sample in nitrogen after the oxide etch and loading it into the vacuum chamber of the evaporator was critical. This time was kept to an absolute minimum. Table 7.3 gives the diode ideality, series

resistance, reverse breakdown voltage and ohmic contact resistance of the diode batches in Table 7.2.

	A_r (μm)											
	16		14		12		10		8			
Batch	η	R_s	η	R_s	η	R_s	η	R_s	η	R_s	V_{br}	R_{oc}
UBD-5	1.26	9.0	1.19	9.0	1.27	12.3	1.17	13.5	-	-	5.1	5.1
UBD-6	1.08	17.0	1.12	15.7	-	-	-	-	-	-	-	5.5
UBD-7	1.19	7.9	-	-	-	-	-	-	-	-	-	5.5
UBD-8	1.10	14.6	-	-	-	-	-	-	-	-	-	5.5
UBD-9	1.17	5.5	1.15	9.3	1.15	9.7	1.16	8.2	1.17	7.9	~10	4.0
UBD-10	1.14	18.1	1.14	12.8	1.15	13.3	1.18	12.8	1.16	13.9	~10	4.5
UBD-11	1.12	14.2	1.12	9.1	1.13	13.0	1.13	17.0	1.13	11.2	~10	4.5
UBD-12	1.12	11.4	1.12	10.9	1.13	12.8	1.08	15.9	1.13	13.9	~10	3.5
UBD-13	1.12	8.4	1.14	15.1	1.07	7.8	1.13	8.5	1.12	5.2	~11	2.5
UBD-14	1.11	6.5	1.06	7.7	1.11	6.4	1.12	7.6	1.12	7.0	~11	3.5
UBD-15	1.11	4.3	1.11	3.6	1.11	4.6	1.11	5.6	1.10	5.6	~11	2.5

Table. 7.3 Showing diode ideality, series resistance, reverse breakdown voltage and ohmic contact resistance for diode batches UBD-5 to UBD-15 using evaporated refractory metals.

The diodes were measured using 2 thin metal probes and a current source. The voltage drop was measured between the probes and no correction for the probe or ohmic contact resistance has been accounted for in the results in Table 7.3. The probe resistance was measured to be about 0.5 Ω in each case, the ohmic contact resistance for each diode batch is included in Table 7.3.

A general trend of increasing diode performance can be seen with the later diode batches, as shown in Table 7.3. Batch UBD-15 displayed most of the characteristics needed for efficient frequency multiplying. The diode ideality and series resistance

for batch UBD-15 was low (if probe resistance is omitted R_s = 3-4 Ω) and these results are comparable to most current research (see section 8.1). The reverse breakdown voltage for diode batch UBD-15 was relatively high, also a requirement for effective frequency multiplying.

Fig. 7.4 is a plot of diode junction capacitance C_j versus applied bias V_b for a 16 μm diameter Ti Schottky diode from batch UBD-15 which also includes modelled predictions of junction capacitance behaviour. Steps were taken during the measurements and plotting to ensure that all parasitic capacitances and any other compensations were accounted for. This included using an open circuit compensation during C/V measurements, subtraction of parasitic capacitance component and compensation for anode enlargement due to under etching of SiO_2. Parasitic capacitance was found to vary between 55 fF for small anodes to 25 fF for large anodes. This effect was due to the generic design of the anode finger used for each diode. A smaller anode would have a higher area of gold finger overhanging the GaAs compared to a larger anode (see section 4.3.3) as the finger dimensions did not change with the anode size. Anode enlargement due to SiO_2 under etching was found to be ~1.3 μm in radius (1 μm of under etching was frequently observed during HF etching of SiO_2). Anode enlargement compensation was confirmed by finding a linear trend in C_j/A_0 for different anodes sizes where A_0 is the anode area. When an enlargement of 1.3 μm was added to the anode radii, the measured C_j/A_0 response was linear. This was confirmed by adding the same factor to the modelled C/V response to give the agreement given in Fig. 7.4.

The measured C/V data was used to check N_D, the epilayer doping concentration, and V_{bi}, the diode built-in voltage, from plotting $1/C^2$ versus V_b and is shown in Fig. 7.5. The gradient of this plot can be used to calculate N_D (see section 4.1) and was found to be 2.2×10^{17} cm^{-3} (wafer actually doped 1.0×10^{17} cm^{-3}). The intercept of the plot is equal to V_{bi} and was found to be 0.79 V which gives a barrier height of 0.83 eV for the Ti-GaAs interface (given as 0.82 eV in [7.6]).

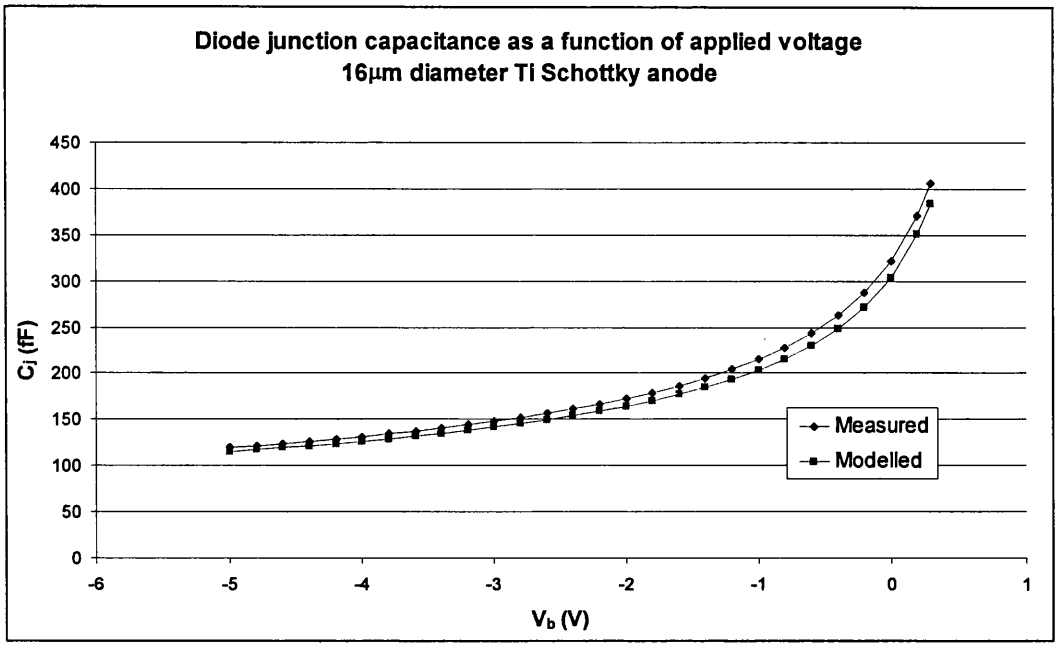


Fig. 7.4 C/V plot for 16 μm Ti Schottky diode from batch UBD-15.

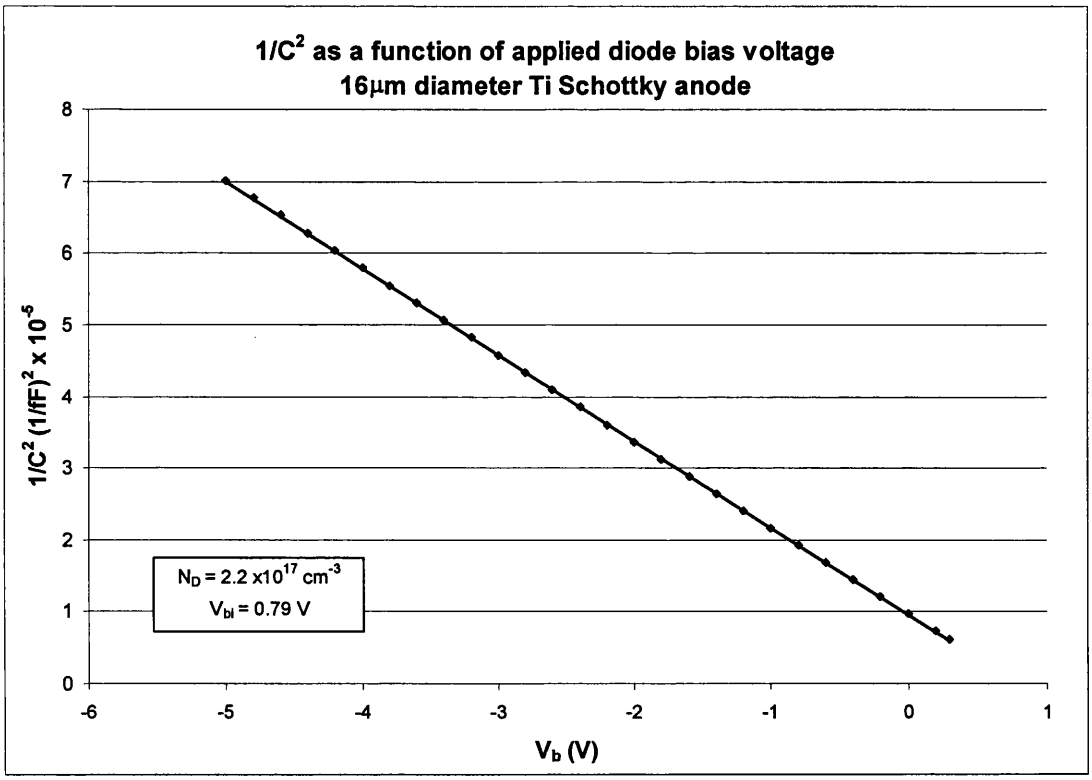


Fig. 7.5 $1/C^2$ versus V_b for 16 μm Ti Schottky diode from batch UBD-15.

The forward current density characteristic for a 16 μm diode from batch UBD-15 is shown in Fig. 7.6. The y-intercept of this graph is equal to the saturation current density J_s which can be used to determine the diode barrier height (see section 4.2.1).

The barrier height was found to be 0.75 eV using this method (a difference of ~9 % which is reasonable giving the much smaller range of voltages that the results are taken over) compared to the value of barrier height found using the C/V method.

An SEM photograph of the test diodes used for diode batches UBD-9 to UBD-15 is shown in Fig. 7.7 with *n* etch and air channel etch (steps 5 and 6 respectively from section 7.1.8).

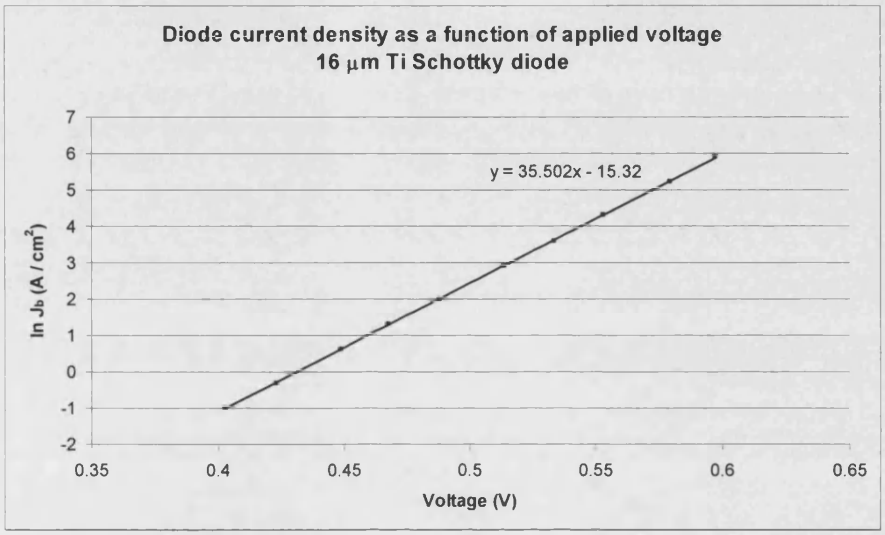


Fig. 7.6 Forwards current density as a function of V_b for a 16 μm diameter Ti Schottky diode from batch UBD-15.

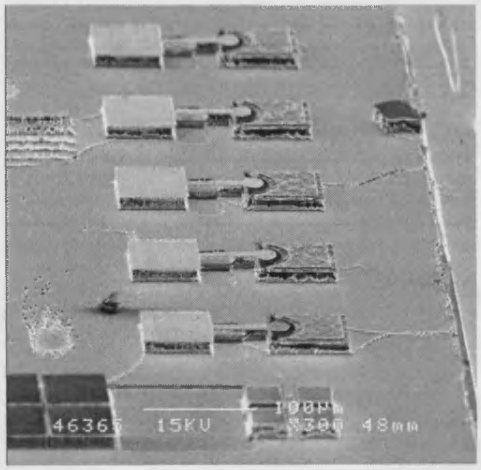


Fig. 7.7 SEM photograph of the test diode structures used for taking I/V and C/V measurements.

7.3 Membrane Structure

The fabrication of the membrane structure was achieved using a combination of dry etching and wafer lapping (steps 7 and 8 in section 7.1.8). The dry etching (also used in step 5 in section 7.1.8) performed on the GaAs samples needed to leave a smooth surface as this would benefit the RF characteristics. The dry etching also had to have relatively good anisotropy so that no under etching of critical areas occurred. Good quality gold films of substantial thickness (> 1 μm) was also an issue covered in this section.

7.3.1 Good Quality Gold Films

It would be expected that RF reflections would occur if non-smooth gold films were used for the metallization of the microstrip, fingers and ohmic capping layers. Since thick gold was needed to reduce the overall resistance of the circuit and as a substantial mask for the dry etching of the *n* and n^+ layers, deposition was performed in the e-beam evaporator. The spitting of the gold during e-beam evaporation resulted from a combination of a polluted gold target, a poorly aligned e-beam filament and a high evaporation rate (>1.0 nm s^{-1}). Lower evaporation rates reduced spitting but lead to machine over-heating. An example of the surface roughness due to spitting can be seen in Fig. 7.8.

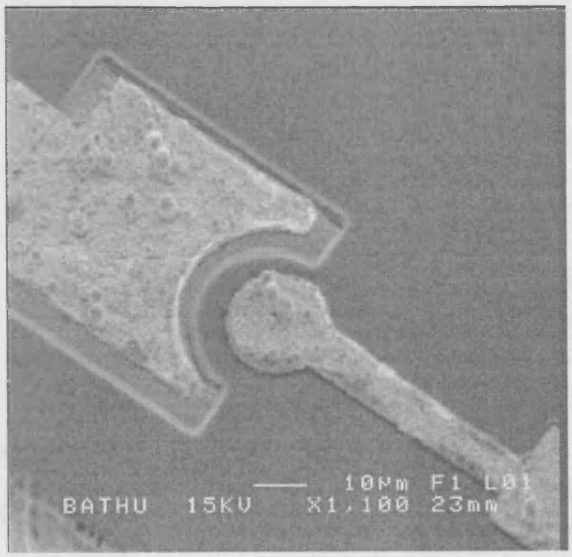


Fig. 7.8 SEM photograph showing the poor quality of the gold capping layer on the anode finger and ohmic contact.

Any temperature increase near or above that of the baking point of the resist (115°C) would render it immoveable and ruin the sample. Allowing the sample and e-beam chamber to cool mid-way through an evaporation was an effective method of overcoming this problem although time consuming. Re-aligning the e-beam filament and using new unpolluted gold in a new crucible overcame 75% of the surface roughness. It was also confirmed that loading 4 boats in the thermal evaporator with the maximum amount of gold could produce much better quality gold films up to approximately 800 nm in thickness.

7.3.2 Smooth Dry Etched Profiles

Initial dry etching was done using chlorine and argon gases which resulted in very rough surfaces as shown in the SEM photograph in Fig. 7.8.

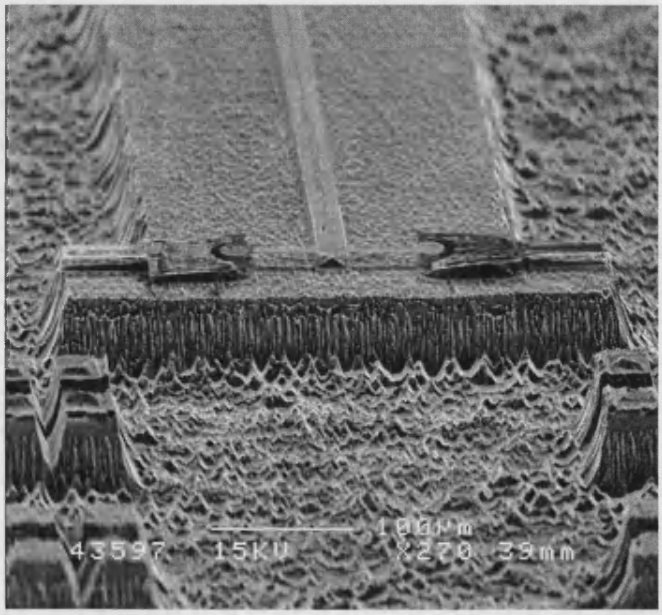


Fig. 7.8 SEM photograph of very poor dry etched surface using chlorine and argon gases.

The problem was alleviated when $SiCl_4$ was used in place of chlorine in the RIE chamber. This resulted in smooth mirror finish to the etch surface and vertical sidewalls. An SEM photograph of a $SiCl_4$ dry etched sample is shown in Fig. 7.9. The last problem encountered with this procedure was the wavy sidewalls resulting from the long exposure needed for the thick resist in step 7 (section 7.1.8). The high dose of UV light on the thick resist resulted in non-uniform resist sidewalls and hence dry etch side walls were directly affected by this. Overcoming this problem

was done by using the SiO_2 as a mask which could be etched neatly using standard thickness resist. Unfortunately a full chip process using this technique was not carried out using the multiplier design. However an SEM photograph of the procedure used on a mixer circuit [7.10] is shown in Fig. 7.10 displaying a very neat sidewall profile.

Fig. 7.9 SEM photograph showing the smoother etched surface of the $SiCl_4$ based RIE.

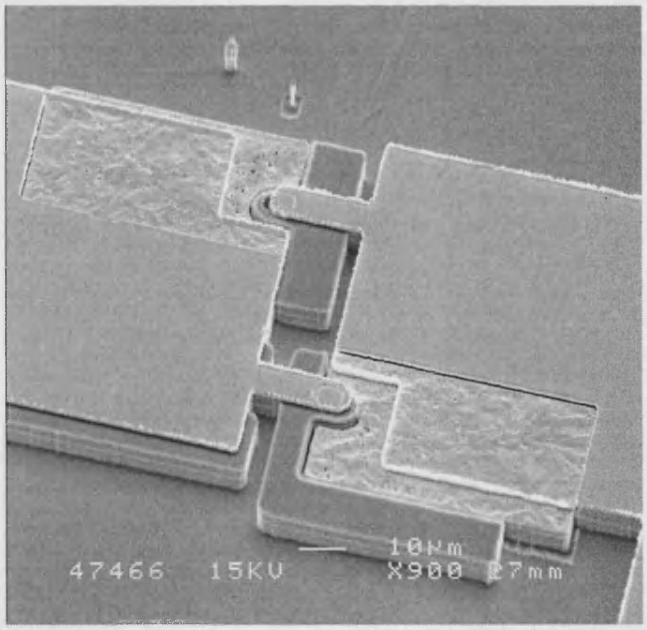


Fig. 7.10 SEM photograph of a mixer circuit with anti-parallel diodes where dry etching has been performed using SiO_2 as the dry etch mask [7.10].

7.3.3 Modified Air Bridge

The air channel wet etch (step 6 section 7.1.8) performed to isolate the diodes proved to be a non-trivial step in the processing. As this step was performed after the dry etching of the n and n^+ layers the sidewalls needed to be protected with resist so the wet etch did not under etch the diodes as shown in Fig. 7.12.

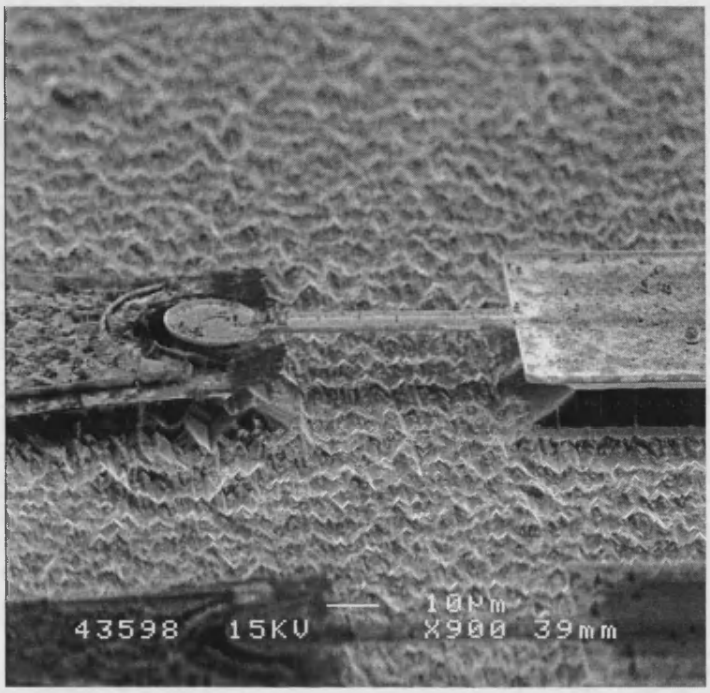


Fig. 7.12 SEM photograph of an under etched diode. Etch profile under the anode pad is correct but severe under etching around the anode has completely eradicated the diode.

Even with resist covering the sidewalls the diodes were still slightly under etching resulting in degradation of diode performance. This problem was rectified by modifying the resist pattern used for the wet etch. Originally windows in the resist were opened above the fingers but the poor adhesion between the SiO2 and the GaAs resulted in a fast etch towards the anodes. Moving the windows in the resist from above the fingers and replacing them with a single window between them gave a much larger under etch buffer (from 5 to >20 μm). This technique meant that the parasitic capacitance of the circuits would be slightly higher but the devices would be isolated. An SEM photograph of the finished multiplier with the shifted air channel etch is shown in Fig. 7.13. Notice the etch profile under the fingers creeping towards the anodes at the $GaAs/SiO_2$ interface. At this stage the multiplier circuits were ready for backside lapping and the entire completed chip is shown in Fig. 7.14. Due

to the overall length of the circuit (nearly 9mm) the membranes suffered severe warping when lapped down too thin. It was found that at 20 μm thickness the membranes bowed to such an extent that they could not be mounted inside the block correctly. 45 μm was found to be the limit of how thin the GaAs could be lapped before warping became a considerable effect.

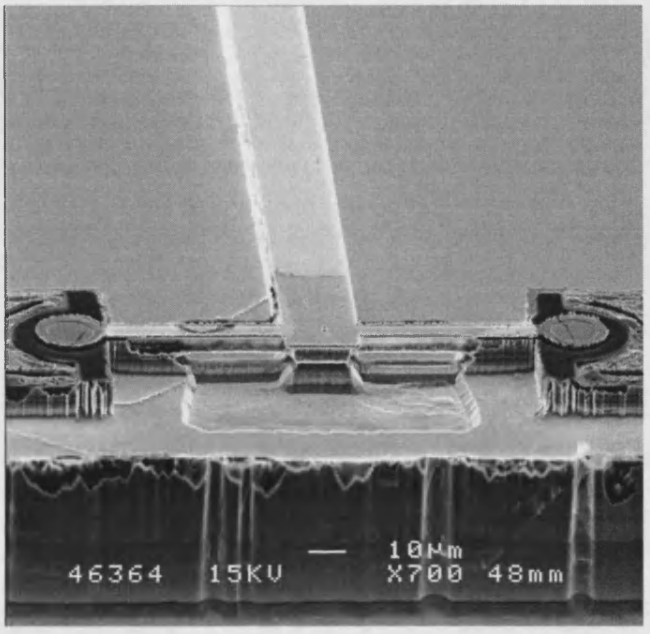


Fig. 7.13 SEM photograph of a completed multiplier structure with shifted air channel to prevent anode under etching.

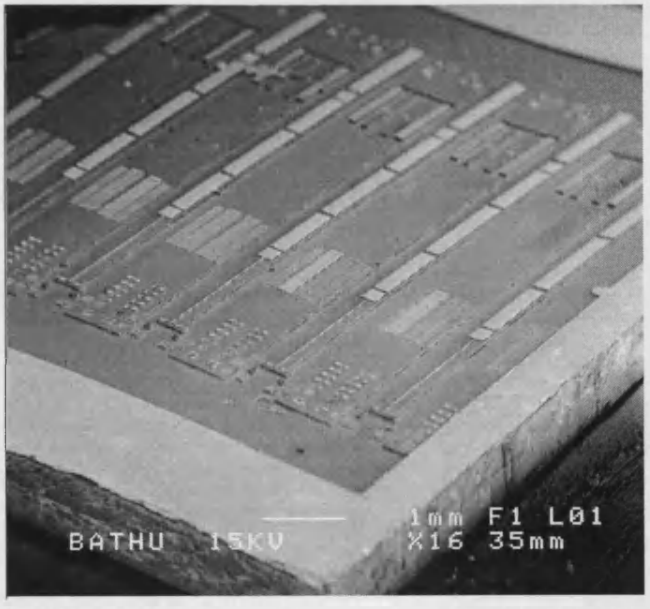


Fig. 7.14 SEM photograph of completed 200 GHz multiplier chip ready for backside lapping.

7.4 Multiplier Block

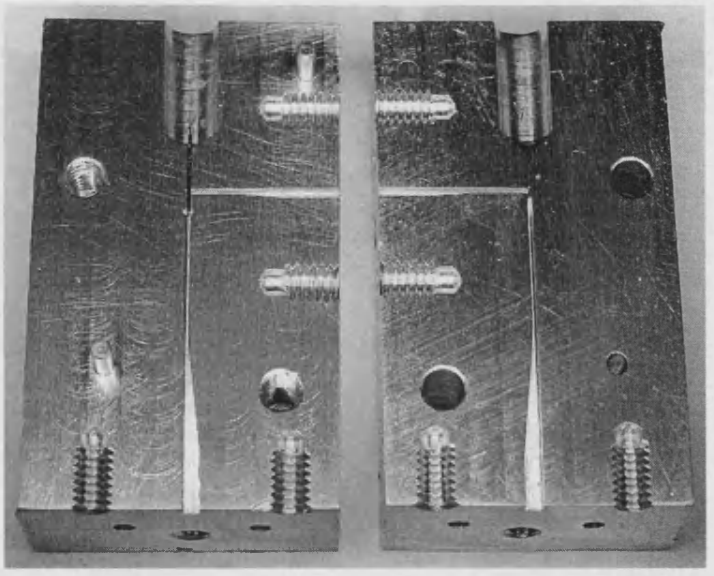
The multiplier block was machined from two parts of brass using a CNC Micromill. Simple coding could be written to control the tiny milling tools used to cut the small waveguide and microstrip channels. Milling tools of sizes 0.80, 0.30 and 0.25 mm in diameter were used in the final construction with a much larger 8 mm bit used for larger operations such as facing-off.

The CNC code had to be written to avoid putting the tiny and fragile milling tools under any undue stress. This meant driving across the working surface slowly and with tiny increments to depth (as little as 30 μm) with the maximum rotation speed (because the milling diameter was so small). This combination of parameters resulted in extremely long machining periods (up to 15 hours continuous machining for a half block).

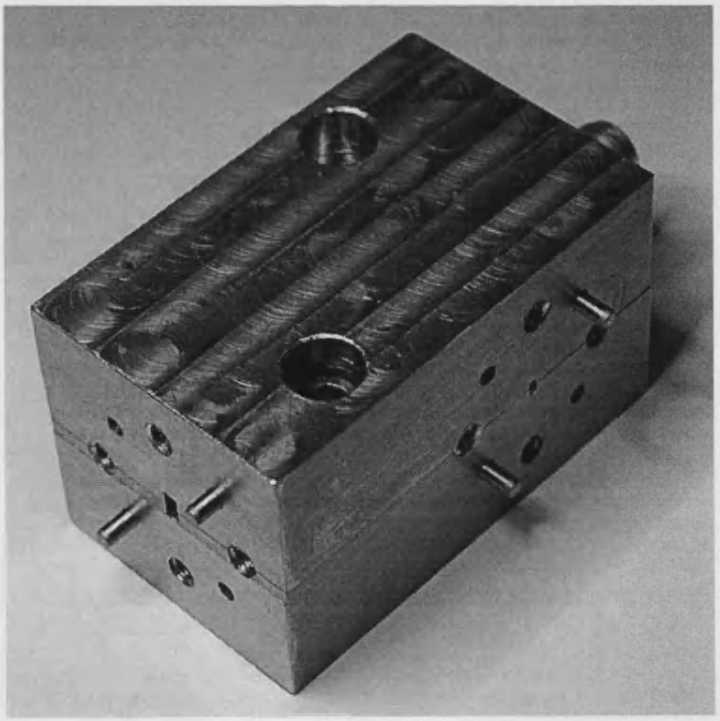
Several generations of block were made improving the alignment of the waveguides to one another in the bottom and top halves of the block. Tiny backlash errors in the mills gearing, causing small but noticeable misalignment, were eliminated by minimising tool cutting paths and driving to reset locations at various points during the program. Waveguide templates were made to align the dowel and bolt holes for the waveguide flanges in the block. These proved to be a very accurate and convenient way of overcoming misalignment to external waveguides. Fig. 7.15 shows some photographs of the final generation multiplier block with (a) a mounted multiplier circuit inside and (b) external view of block halves bolted together.

Mounting the multiplier circuit inside the block was quick and easy with even limited experience and achievable with the most basic tools. A single membrane could be picked up using the surface tension of IPA on the end of a thin non-metallic rod and simply dropped into the block. Held in place with a small amount of super glue near the DC end of the circuit, where its effects will be non-existent to the RF circuit, the tabs either side of the diodes could be electrically contacted to the waveguide walls using a silver-based conducting epoxy. The DC connection was made by similarly contacting a small gold wire from the end of the RF filter to the small (SMA) coaxial feed through the rear of the block. After a single diode was contacted to the waveguide walls the IV characteristics were measured. When the second diode was

successfully contacted the IV response corresponding to an anti-series pair of diodes was observed. This was an excellent way of determining circuit continuity as visual inspections were mostly unreliable.



(a)



(b)

Fig. 7.15 Photograph showing multiplier block split in half with multiplier circuit inside and (b) block closed showing WR10 and WR5 waveguide flanges and SMA connector ready for testing.

References – Chapter 7

[7.1] D. W. Shaw, "Localized GaAs etching with acidic hydrogen peroxide," *J. Electrochem. Soc.*, vol. 128, no. 4, April 1981, pp. 874-880.

[7.2] K. R. Williams, R. S. Muller, "Etch rates for micromachining processing," *Journal of Microelectromechanical Systems*, vol. 5, no. 4, December 1996, pp. 256-269.

[7.3] M. B. Stern, P. P. Liao, "Reactive ion etching of GaAs and InP using $SiCl_4$," *Journal of Vacuum Science and Technology*, vol. 1, no. 4, 1983, pp. 1053-1055

[7.4] N. Chand, *et al.*, "Molecular beam deposition of high quality silicon dioxide dielectric films," *Journal of Crystal Growth*, vol. 148, no. 4, March 1998, pp. 336-344.

[7.5] M. I. Alayo, *et al.*, "Thick SiO_xN_y and SiO2 films obtained by PECVD technique at low temperatures," *Thin Solid Films*, vol. 332, no. 1, November 1998, pp. 40-45.

[7.6] R. Williams, "Modern GaAs processing methods," Artech House, Inc. 1990.

[7.7] F. A. Perez, A. Singh, G. Aroca, "High temperature I-V characteristics of the as-deposited and thermally annealed W/n-GaAs Schottky junctions fabricated by RF sputtering," Devices, Circuits and Systems, *Proceedings of the 1998 Second IEEE International Caracas Conference*, 2-4 March 1998, pp. 79-82.

[7.8] C. A. St. Jean, *et al.*, " Novel fabrication of Ti-Pt-Au/GaAs Schottky diodes," *IEEE Transactions on Electron Devices*, vol. 47, no. 7, July 2000, pp. 1456-1468.

[7.9] R. J. Morrissey, "Platinum plating," *Metal Finishing*, vol. 98, no. 1, 2000, pp. 291-291.

[7.10] J.-M. Rollin, Private communication.

Chapter 8

Testing and Results

This chapter contains a summary of the DC results for the highest performance diodes fabricated during this project. An SEM photograph of the final multiplier circuit used for testing and photographs of the final multiplier block are included. RF experimental setup is included and multiplier performance results are given. A comparison between measured and modelled multiplier performance and quantitative multiplier results are given.

8.1 Schottky Diode Results

Diodes were tested using a standard two probe method with 5 um tipped gold probes. A Labview environment was used to control a Keithley 220 current source and a Keithley 617 electrometer. Diode I/V measurements were recorded from 1 uA to 1 mA and repeated 20 times for each diode (allowing the diode to stabilise and eliminate any charging effects), averaging the results. Reverse breakdown voltage was measured at 1 mA reverse current. Barrier height was measured using the C/V extrapolation method from section 4.1.

Table 8.1 gives a summary of the best performing diodes that were fabricated during this project. These diodes are well suited to multipliers for a number of reasons;

- Low series resistance results in more power delivered to the diode junction where it can be converted to the higher harmonic(s).
- Low ideality which was stable over long periods of testing implying a good, near defect free interface between metal and GaAs.
- High breakdown voltage giving the multiplier a broad range of bias voltage.

Fig. 8.1 displays a plot of the I/V characteristics for the 14 um Ti Schottky diode from batch UBD-15 including the breakdown profile. Fig. 8.2 is a plot of the measured and modelled forward I/V response from the same diode. Fig 8.3 is the

C/V response of the same diode and the modelled comparison is plotted for reference. In both Fig. 8.2 and Fig. 8.3 there is excellent agreement between modelled and measured results.

Extreme care was taken to reduce contamination of the diodes *n* GaAs surface before anode deposition. A thick gold capping layer helped to reduced series resistance. The consistency of diode performance across the entire device sample was cornerstone to the success of these diodes. This can be partially attributed to using evaporated titanium as the anode material and in the rigorous sample preparation. Table 8.1 gives a summary of the best diode characteristics produced during this project, (any resistance or capacitance in any cables used to take the results have been accounted for). Table 8.2 shows DC diode characteristics for some state-of-the-art Schottky diodes produced using a similar processing technique by leading researchers in the field. Diodes produced in this project are comparable to those of leading research.

Batch	A_r	t_e (um)	N_D (cm^{-3})	Φ_b	η	R_s (Ω)	V_{br} (V)	C_{j0} (fF)	C_p (fF)
UBD-15	12	1.0	10^{17}	0.81	1.11	4.1	11.3	195	52
UDB-15	14	1.0	10^{17}	0.83	1.11	3.1	11.6	267	45
UBD-15	16	1.0	10^{17}	0.83	1.11	3.8	11.4	321	25

Table 8.1 Summary of state-of-the-art diode characteristics fabricated during this project.

Diode Type or Structure	A_r (μm)	t_e (μm)	η	R_s	V_{br}	Ref.
Ti/Pt/Au	1	-	1.40	13.0	-	[8.1]
Ti/Au	0.9	-	1.13	10.0	-	[8.2]
Ti/Pt/Au	1.4	0.1	1.19	4.9	-	[8.3]
Ti/Pt/Au	6	1.0	-	12.6	17.5	[8.4]
Ti/Pt/Au	6	0.4	1.12	4.6	10.6	[8.5]
QVD	-	-	1.05	3.0	-	[8.6]
UVa-SB13T1	13	-	-	1.2	14.0	[8.7]

Table 8.2 Comparing DC characteristics of some state-of-the-art Schottky diodes.

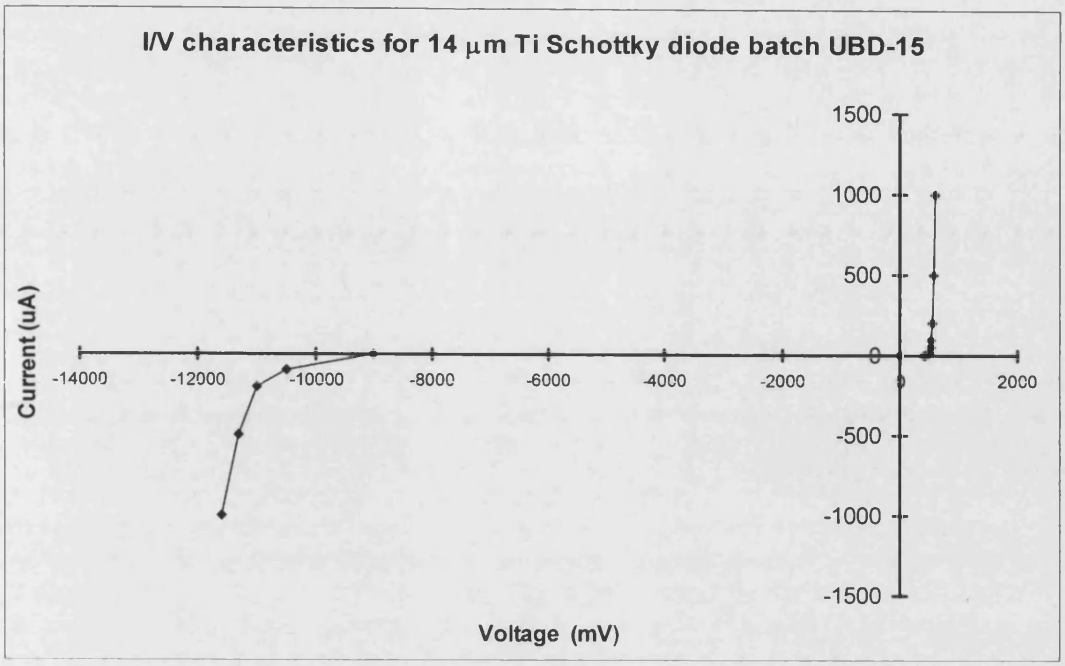


Fig. 8.1 Showing the measured I/V plot of the 14 μm diode Ti Schottky varactor diode from batch UBD-15.

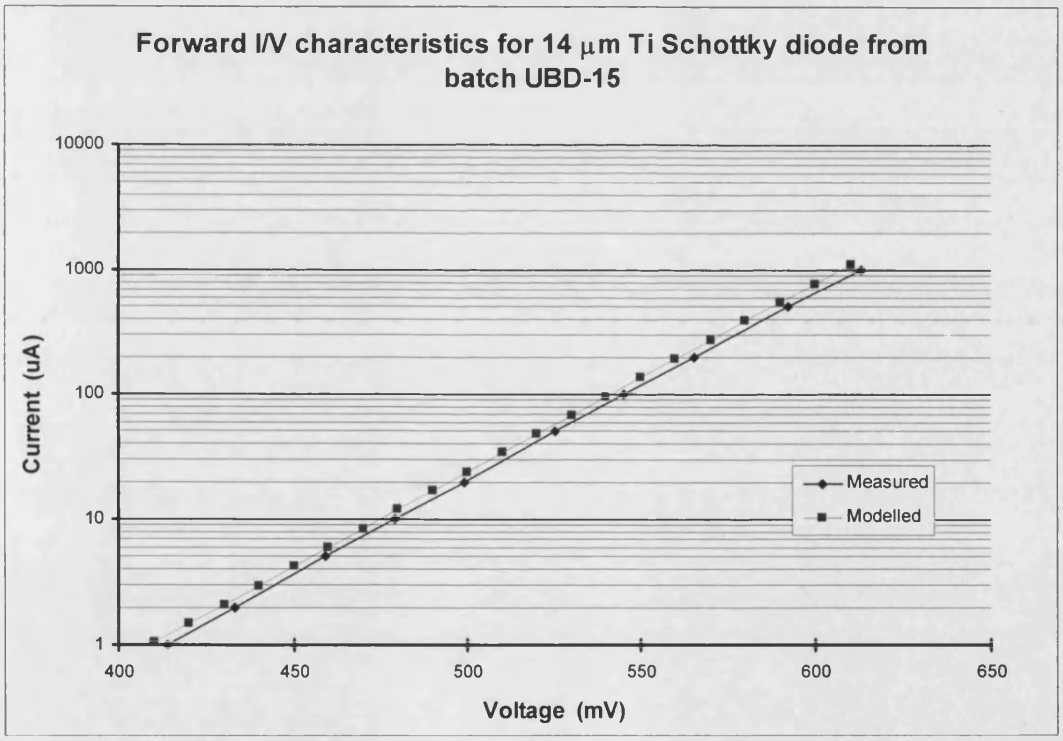


Fig. 8.2 Showing comparison between measured and modelled forward I/V characteristics of the 14 μm Ti Schottky varactor diode from batch UBD-15.

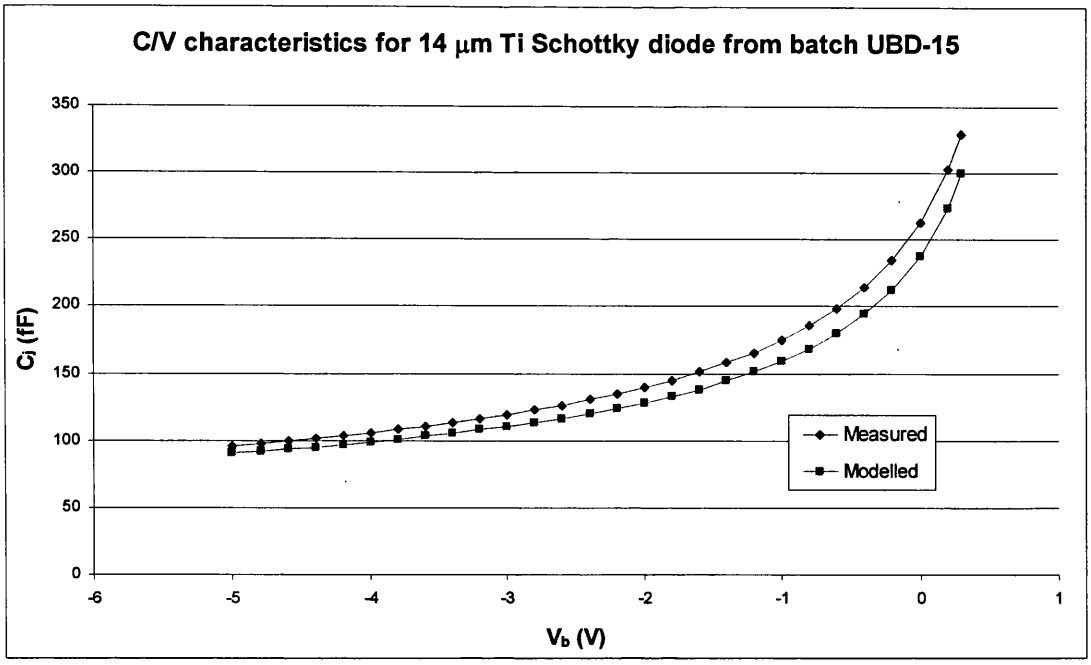


Fig. 8.3 Showing comparison between measured and modelled C/V characteristics of the 14 μm Ti Schottky varactor diode from batch UBD-15.

8.2 Processing Results

8.2.1 Semiconductor Processing

Processing work was completed in the David Bullet Laboratory and the Terahertz Technology Laboratory. Major processing issues were divided between achieving smooth dry etch profiles and uniform smooth gold transmission lines. Using $SiCl_4$ and argon gases during the reactive ion etching dramatically improved the dry etched surface. Gold films deposited using a thermal evaporator gave much better film quality than those deposited using an e-beam evaporator. Problems were encountered using thick photoresist resulting in 'wavy' dry etched sidewalls. This effect was overcome as shown in section 7.3.2. SEM photographs of the final multiplier circuit are shown in Fig. 8.4 and Fig. 8.5.

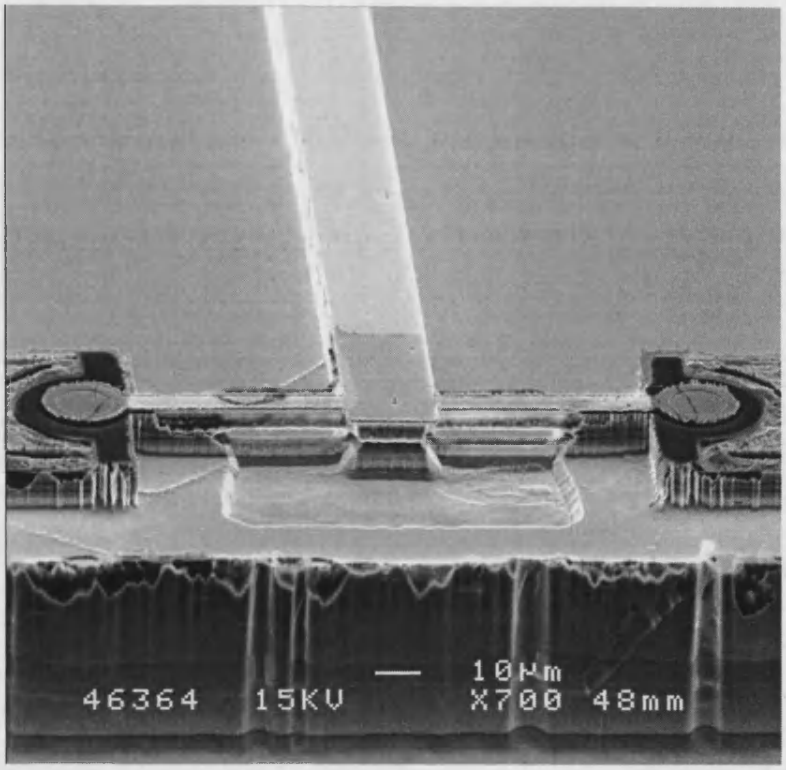


Fig. 8.4 SEM photograph of the diodes, the air channel, the gold anode fingers and the microstrip transmission line.

Fig. 8.5 SEM photograph showing the 45 um deep T-etch defining the membrane outline of the finished multiplier circuit.

8.2.2 Multiplier Block

The multiplier block was fabricated using a mill with milling tools as small as 0.25 mm in diameter. The cutting tolerances of the machine were very good but minor backlash in the gearing resulted in waveguide misalignment in early prototypes. By driving the cutting tool to certain reset locations the backlash could be eliminated and accurate alignment between the top and lower block achieved. The final block used for testing is shown in Fig. 8.6, Fig. 8.7 and Fig. 8.8. Images showing the DC connection of the 17 μm gold wire to the SMA connector and the connection of the diode tabs to the waveguide walls with the silver epoxy paint are shown in Fig. 8.9(a) and (b) respectively.

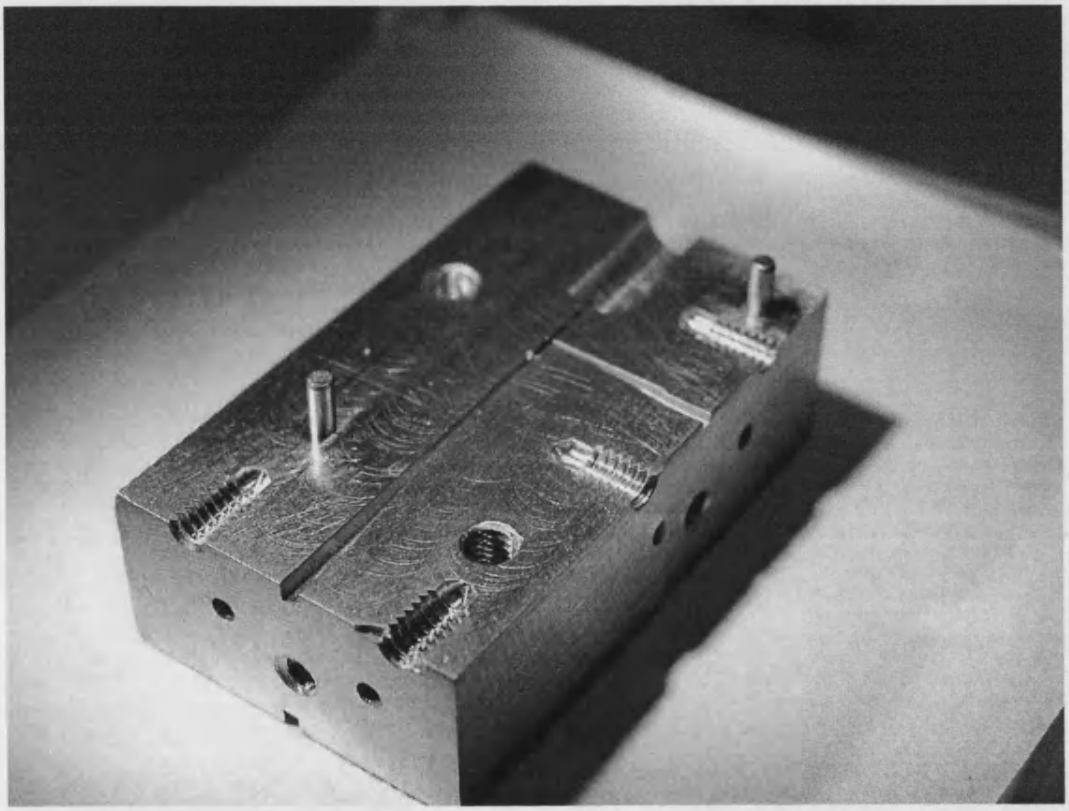


Fig. 8.6 Lower block containing half of the input and output guides, the suspended microstrip cavity and the dowel pins for alignment to the upper block.

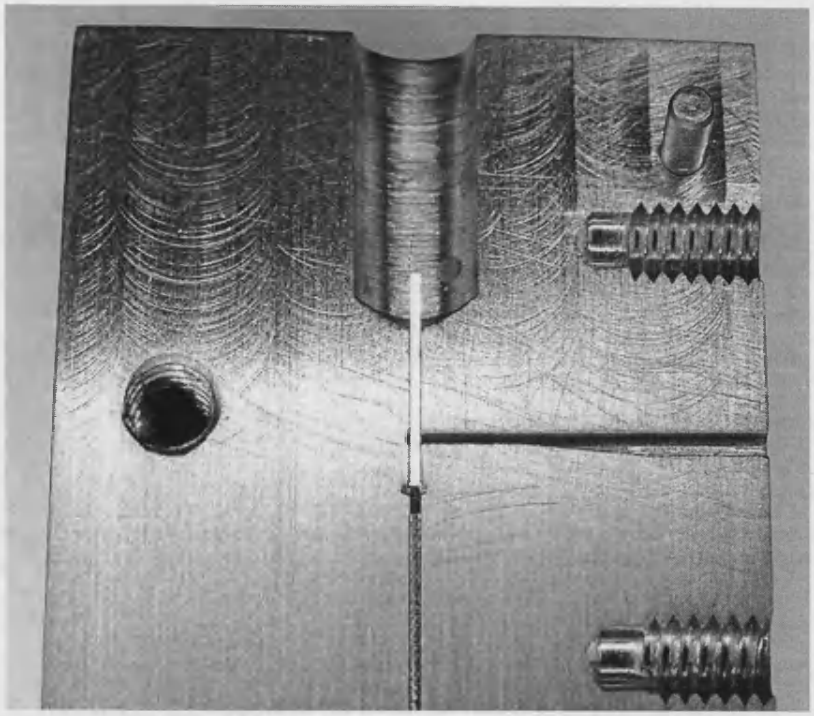


Fig. 8.7 Closer view on the lower block with a multiplier circuit mounted in the suspended microstrip cavity. The multiplier membrane substrate protrudes into the DC bias chamber where an external connection was made to the end of the filter metallization used for applying a voltage bias to the diodes.

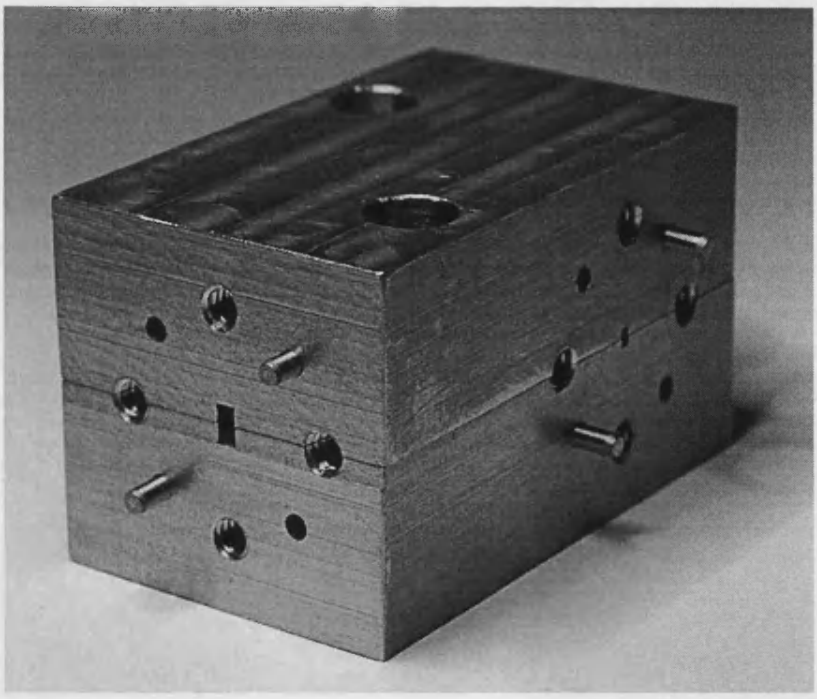
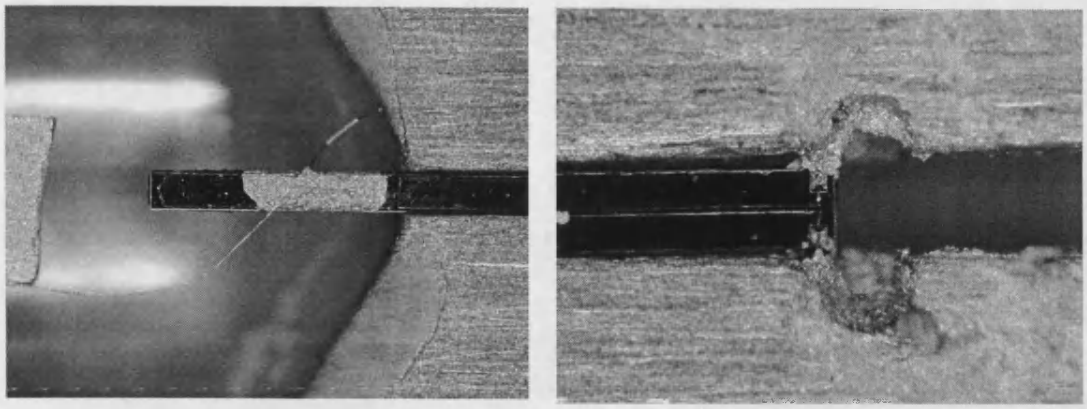


Fig. 8.8 Complete multiplier block with upper half accurately aligned to the lower half and securely joined with two large bolts (counter-bores visible in the upper block where bolt head are located). Entire block size measured approximately 45 x 35 x 35 mm.



(a) (b)

Fig. 8.9 Showing (a) the 17 μm diameter gold wire used to connect the SMA pin to the end of the microstrip on the 45 μm thick GaAs membrane and (b) the silver conducting paint used to electrically contact the diode tabs to the waveguide walls.

8.3 Multiplier RF Results

A schematic diagram of the experimental setup used to test the multiplier is shown in Fig. 8.10. A Klystron powered with a 2.5 kV source was used to produce fundamental power in the frequency band 95 – 110 GHz. Part of this power was fed to a harmonic mixer where it was mixed down with an LO (Local Oscillator) source (~10 GHz) to produce an output near 1 GHz (termed the IF or Intermediate Frequency). The output could be easily read on a spectrum analyser and the input frequency calculated by summing the 10^{th} harmonic of the LO with the IF. It was essential to know the input frequency accurately as the output frequency would be exactly double that of the input. A -10 dB directional coupler was used directly before the input guide to gauge a relative power level available to the input circuit of the multiplier. A power detector was attached directly to the output of the multiplier and 10 V DC power supply was connected to the SMA terminal at the rear of the block. The klystron could be tuned in frequency and the input (and therefore output) frequencies monitored on the spectrum analyser.

Power was seen at the output of the multiplier and the results are shown in Fig. 8.11. The measurements shown in Fig. 8.11 were taken without using the DC bias as problems were encountered with the source or set up. The modelled output spectrum in Fig. 8.11 was taken using no bias and resulted in a shift in the peak output by 2 GHz to 196 GHz. Power measurements are given relative to the modelled data as

power detectors were not calibrated. Results taken from the power detectors were DC voltages so no direct comparison to the modelled power levels could be made. The results do, however, show a fair comparison between the modelled and measured output spectrum shape and the peak output frequency.

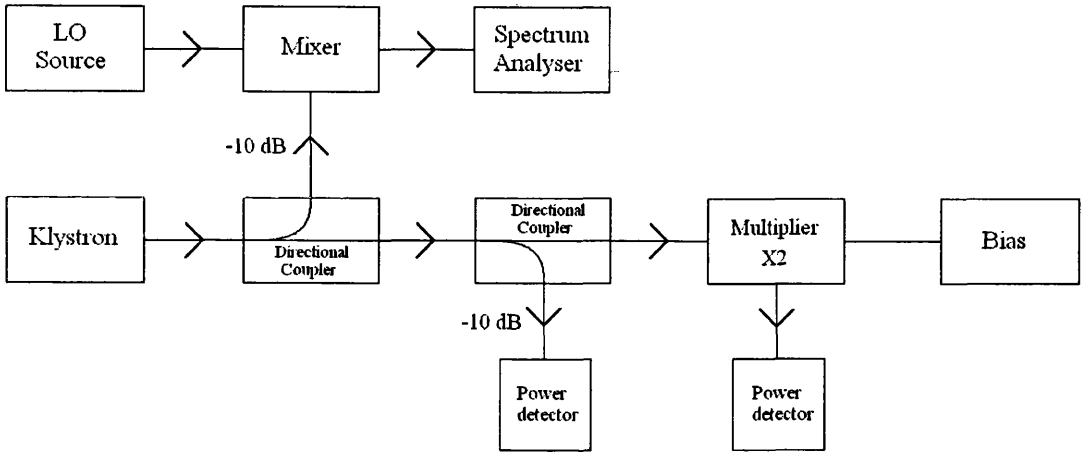


Fig. 8.10 Schematic of experimental setup used for RF testing of the multiplier.

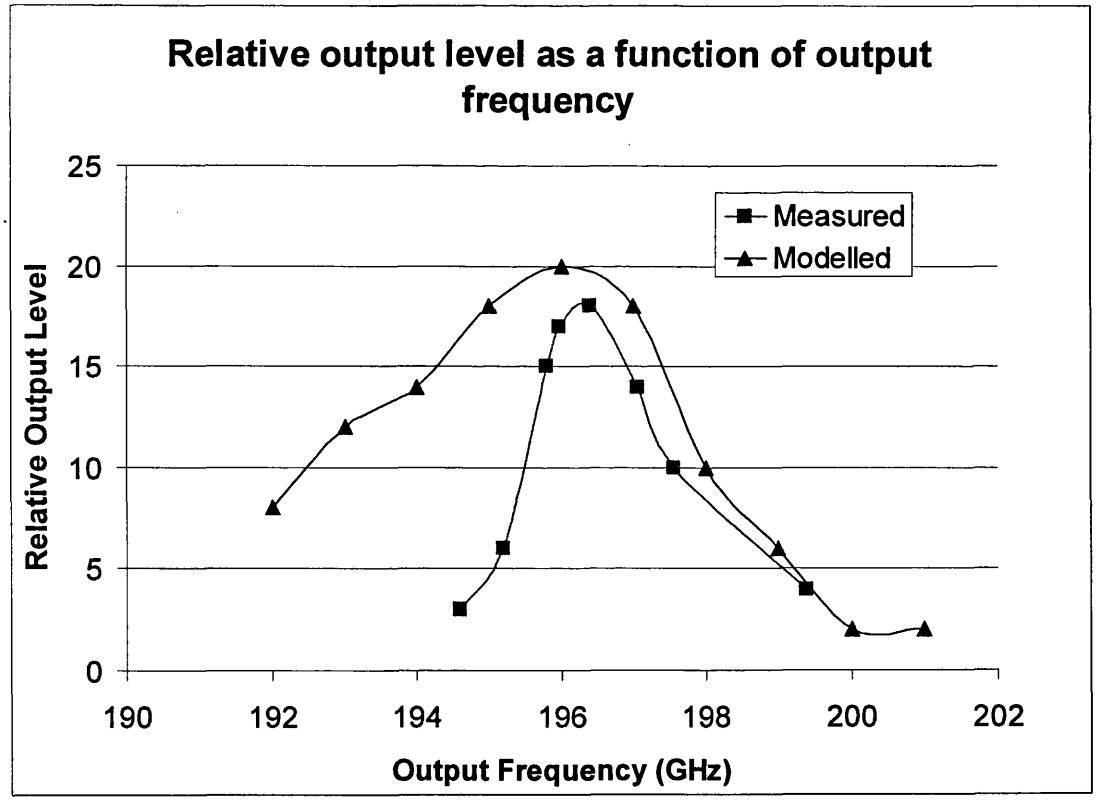


Fig. 8.11 RF response of the multiplier circuit using zero bias. Measured power levels are relative to the modelled data as no power detectors were calibrated.

Quantitative measurements of multiplier performance were taken at the Rutherford Appleton Laboratory (RAL) in Didcot. Using a BWO G4-141dM (GPIB) mm-wave source and mm-wave power meter, readings of output power and efficiency were taken.

Due to poor calibration of the equipment prior to measuring, an output spectrum as a function of frequency could not be determined accurately. However, with an input power of approximately 50 mW the multiplier produced a peak output power of 0.10 mW compared to 0.7 mW predicted with the advanced multiplier model. The conversion efficiency was measured at approximately 0.2 % and predictions using the advanced multiplier model put this figure at 1.4 %.

However, predictions of multiplier performance were made using a reverse voltage bias across the diodes of anything up to 12 V. When using the advanced multiplier model with 50 mW input power and -2 V bias (a bias of 0 V was not included in the multiplier program) the predicted peak output power was 0.4 mW and peak efficiency was 0.8 % showing a little improvement in the correlation between measured and modelled data. A summary of all predicted and measured results of the 200 GHz suspended membrane frequency multiplier are shown in Table 8.3.

	Basic Model Predictions		**Advanced Model Predictions**			**Measured Results**
Input Power (mW)	250	50	250	50	50	50
Diode Bias Applied	yes	yes	yes	yes	no	no
Peak Output Power (mW)	57	4.4	12	0.7	0.4	0.1
Peak Efficiency (%)	22	8.8	4.6	1.4	0.8	0.2

Table 8.3 Showing a summary of all predicted and measured multiplier performance for the 200 GHz multiplier.

References – Chapter 8

[8.1] I. Mehdi, P. Siegel, M. Mazed, "Fabrication and characterization of planar integrated Schottky devices for very high frequency mixers," High Speed Semiconductor Devices and Circuits, *Proceedings IEEE/Cornell Conference on Advanced Concepts*, 2-4 August 1993, pp. 94-102.

[8.2] S. M. Marazita, *et al.*, "Integrated GaAs Schottky mixers by spin-on-dielectric wafer bonding," *IEEE Transactions on Electron Devices*, vol. 47, no. 6, June 2000, pp. 1152-1157.

[8.3] I. Mehdi, *et al.*, "Planar GaAs Schottky diodes integrated with quartz substrate circuitry for waveguide subharmonic mixers at 215 GHz," *Microwave Symposium Digest*, IEEE MTT-S International, vol. 2, WE2E-5, 23-27 May 1994, pp. 779-782.

[8.4] J. W. Archer, R. A. Batchelor, C. J. Smith, "Low-parasitic, planar Schottky diodes for millimeter-wave integrated circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 38, no. 1, January 1990, pp. 15-22.

[8.5] C. A. St. Jean, *et al.*, "Novel fabrication of Ti-Pt-Au/GaAs Schottky diodes," *IEEE Transactions on Electron Devices*, vol. 47, no. 7, July 2000, pp. 1456-1468.

[8.6] C-I. Lin, *et al.*, "Planar Schottky diodes for submillimeter wave applications," *Terahertz Electronics Proceedings*, IEEE Sixth International Conference, 3-4 September 1998, pp. 135-138.

[8.7] D. W. Porterfield, *et al.*, " A high-power fixed-tuned millimeter-wave balanced frequency doubler," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 4, April 1999, pp. 419-425.

Chapter 9

Conclusions

9.1 Schottky Diodes

A variety of methods were attempted in developing Schottky diodes with low ideality and low series resistance. Methods involving evaporating metals such as gold (section 7.2.2.1) and silver (section 7.2.2.2) produced diodes that gave poor results. Electroplated platinum anodes (section 7.2.2.3) gave promising results but could not deliver the uniformity and yield needed for this project. With improved electroplating equipment some of these problems could be alleviated but stability in the I/V characteristics of these devices was also of concern. Diodes made with sputtered tungsten anodes (section 7.2.2.4) seemed to come second in performance to the evaporated refractory metal anodes (section 7.2.2.5). The stability of diodes with sputtered tungsten anodes was not matched with any other fabricated diode. This could be related to the UHV system dedicated to depositing tungsten and less likely to incur contamination. This is dissimilar to the e-beam evaporator which was used for many different metals by a greater number of users and likely to incur more contamination. It is believed that further work concentrated on sputtered tungsten anodes with thicker gold capping layers could equal or exceed their evaporated refractory counterparts.

However, evaporated titanium anodes with thick gold capping layers proved to produce the best all-round diodes. Processing recipes were fine tuned to give low ideality, low series resistance and a high breakdown voltage essential for efficient frequency multiplying. As the thickness of the gold capping layer seemed to have a direct effect on the properties of the diode (i.e. R_s) it is believed that an electroplated gold layer > 1 um may increase the performance of these devices further.

Poor adhesion at the SiO_2/GaAs interface produced many problems during processing and the failure of many devices. SiO_2 removal during exposure to HF led to severe under etching. These effects were compensated with sample dehydration, adhesion promoter, and in some cases post baking the resist. Dry etching of the SiO_2

could overcome some of these problems including anode enlargement caused by wet etching in HF. However, dry etching can cause damage to the surface of the *n* GaAs material due to the high energy ions inside the RIE system. A likely solution would be a combination of part dry etching and finishing with a minimal amount of HF wet etching.

Measured diode DC characteristics gave excellent correlation with predicted values and the results can be seen in section 8.1. Extracted values of N_D and Φ_b from I/V and C/V data were close to those expected. A comparison of Ti Schottky diodes DC characteristics from batch UBD-15 against diodes produced by other researchers is given in section 8.1. Diodes produced in this work were comparable to those of other leading research groups.

9.2 Membrane Structure

Problems with depositing thick gold layers without surface deformation were overcome. Small irregularities in the transmission lines of the multiplier circuit could lead to minor reflections and introduce unwanted loss in to the multiplier system. Re-aligning the e-beam evaporator filament and using unpolluted gold in a new crucible dramatically improved film quality. High deposition rates resulted in higher levels of metal spitting and hence a reduction in film quality. Using slower evaporation rates led to extended evaporation times and hence the need for cooling periods between evaporations. This added to the overall fabrication process time.

Thick gold layers up to 800 nm could be successfully deposited using a thermal evaporator with excellent film quality. To increase the thickness above 800 nm using a thermal evaporator meant reloading which again required more time.

Again, the adoption of a high quality electroplating system could be a solution. With the correct equipment and knowledge gold layers over 4 um in thickness could be evenly deposited on a sample surface. Seeding the sample by evaporation and using thick photoresist would be an answer to these processing problems. This would also

reduce the resistance of all metal contacts and transmission lines on the circuit, fractionally reducing overall losses.

Of much concern during the processing was the need for smooth dry etched GaAs surfaces. Etch rates with chlorine gas were good but the results were unacceptable (see section 7.3.2). Using $SiCl_4$ and Ar based dry etch recipes with the correct power and pressure levels resulted in mirror-like finishes to the GaAs etched surface. It was also important that the temperature of the sample did not rise above that required to burn the photoresist (> 100°C). Power levels had to be carefully selected to avoid this scenario during the long (up to 3 hours) etches.

Exposing thick resist to the required dose resulted in non-straight sidewalls. This resulted in an etch profile matching that of the resist due to the high anisotropy of the $SiCl_4$ dry etch. Although no multiplier circuits were made using SiO_2 as an etch mask the concept was proven to overcome this unwanted effect and images are shown in section 7.3.2. By masking the area required in standard thinner resist the SiO_2 could be etched around the device and removed, which left the SiO_2 in the outline of the original mask. The selectivity between SiO_2 and GaAs is very high during dry etching, meaning that several microns of GaAs could be etched before the material under the SiO_2 was at risk. This resulted in much straighter sidewalls and could be easily implemented into the processing of this multiplier circuit.

Under etching of the devices during the air channel formation was a product of mask design infancy and poor adhesion at the SiO_2/GaAs interface. The photomask used for all the photolithography (see section 7.1.2) was designed with a 5 um GaAs under etch buffer for the wet etch of the air channel. This meant, in theory, that a GaAs wet etch could be performed for a period of time equal to 5 microns of etching. In theory, only three minutes of GaAs wet etching was needed to produce the air channel. Dramatic under etching of the diodes, as shown in section 7.3.3, meant a modification to this process. It was evident that allowing the sidewalls to be exposed during the wet etching had to be avoided. Modifying the process to allow only a small area to be exposed during the wet etching gave the device isolation without any

damage to the diodes. An SEM image showing the multiplier circuit produced using this modified process is found in section 8.2.

Lapping down the substrate (step 8, section 7.18) was a relatively straightforward task although care had to be taken mounting and monitoring the sample. When mounting the sample it was imperative that the backside sample surface was as parallel to the glass carrier as was possible to achieve. A variation of anything > 25 um could have disastrous effects, removing too much material and ruining the sample. Levelling was achieved by heating the wax and applying physical downward pressure to high areas until the surface profile varied by < 10 um. Etch rates while lapping varied widely and it was important to monitor the last few 100 um carefully. Problems did occur with warped/bowed samples that had been lapped too thin. The optimum membrane thickness was found to be 45 um.

9.3 Multiplier Block

The programming language for the CNC Micromill was simple to implement into the multiplier block design. The work piece had to be moved slowly against the cutting tool to reduce the pressure exerted on the bit which could lead to snapping or bending. Cutting depths were also minimised for the same reasons. Driving to reset locations during cutting minimised backlash errors and improved waveguide alignment between block halves. The long programs often led to overheating of the machine remedied with cooling breaks every few hours.

Mounting the multiplier circuit inside the block was relatively simple. Contacting the diodes to the waveguide walls with the conducting epoxy was a little more challenging but easily confirmed with I/V measurements. The multiplier membranes were very fragile and due to their length were very easy to break. However, in comparison to flip-chip bonding a much smaller device onto a substrate this method was very quick and easy.

9.4 RF Results

The RF measurements of the frequency multiplier showed a fair comparison to predicted values. The measured output spectrum and bandwidth was similar to what was predicted using the advanced multiplier model. The location of the peak in the output spectrum with respect to frequency differed by only 0.4 GHz between predicted and measured results as shown in section 8.3. Assuming this error is entirely due to misalignment of the diodes in the input waveguide the magnitude can be calculated. A shift in output frequency from 196 GHz (modelled) to 196.4 GHz (measured) is equal to a shift in L_{eff} by just 1.9 μm. The cutting tolerances of the mill used to construct the multiplier block were approximately ± 25 μm which corresponds to a potential shift in frequency by up to 2.7 GHz. Little error in the shift in the frequency peak can be attributed to the fabrication of the multiplier membrane circuit. Photolithographic tolerances were of the order of ± 1 μm per step and could not total more than ± 3 μm for the entire process. This would result in a shift in frequency up to 0.3 GHz.

A factor of four can clearly be seen between the predicted and measured peak output power levels shown in section 8.3. The possible causes of power loss in the multiplier are numerous. A possible cause of power reflection seen at the diodes in the input waveguide could appear due to the notches in the waveguide walls used to support the membrane. Examining the S_{11} of the input port of the multiplier would be a simple test to prove or disprove this theory. The inability to seal the two halves of the multiplier block together as they were intended was a possible cause of major power loss at the output. Small amounts of superglue on the surface of the block, as shown in section 8.2.1, resulted in a small fracture through the E-plane of the block. This small gap was probably large enough to leak some power at 200 GHz although no test was done to confirm this. A measurement of the power loss through the DC terminal was also not undertaken. Power loss through the RF filter could be considerable if the filter was not operating correctly. No test was performed to measure power loss through the RF filter due to time limitations. Finally the parasitic capacitance, C_P, of the diodes used in the final multiplier assembly were not measured. Test diodes on the same chip were measured with relatively low C_P

although any inhomogeneity in the wet etching of GaAs may have resulted in a higher C_P on some devices.

9.5 Future Work

9.5.1 Current Project

A key area of development for this project could include an advanced electroplating system for depositing thick gold layers for RF transmission lines and filter structures. Evidence has been gathered that increasing the thickness of the gold capping layer on ohmic contacts and anode fingers greatly reduces the series resistance of the diodes. Using thick photoresist and an advanced electroplating system, gold could be deposited ≥ 4 μm in thickness which would reduce overall losses in the circuit.

A huge step towards reducing overall parasitic losses would come from removing all unwanted n and n^+ material on the GaAs substrate and adopting a mesa-style planar process as demonstrated by Martin *et al* [9.1]. This would eliminate the need for any air channel etching or long dry etches that are currently employed. This would eliminate any capacitive effect that arises between the gold transmission lines and the n/ n^+ layers separated by the thin SiO_2 layer. Furthermore, good devices could be no longer ruined through under-etching at the SiO_2/ n-GaAs during the wet etch of the air channel (section 7.3.3) resulting in huge savings in time and effort.

A more adventurous approach to reducing R_s could be taken as described by Lin *et al* [9.2]. The idea of back-side ohmic contacts originates from the whisker contacted diodes and is therefore not a novel concept. Demonstrating this in a planar process, however, would be slightly more difficult but possible with the photomask used in this project. The reward for achieving this complex procedure would yield a possible reduction in R_s of approximately 0.5 – 1.0 Ω.

Dry etching of the SiO_2 needed for anode formation would be required if better defined anode sizes were to be achieved. Damage caused to the n-GaAs from dry etching the SiO_2 could be avoided through a series of small tests that would result in determining a dry etch time that would remove 90% of the SiO_2, the final part being

removed by wet etching in HF. This would result in a more controllable anode area and hence $C_{j0} + C_j$ would be more predicable giving a better agreement between measured and modelled multiplier performance.

Also included on the photomask for this project was a 4-diode multiplier. Using two pairs of diodes in an anti-series configuration has several advantages including reduction of C_P and higher power handling. Fabricating this circuit would only be advantageous if input power at a suitable level could be sought. A more advanced HFSS model and harmonic balance code would have to be implemented here to determine the optimum value of L_{eff}. This would imply using a more sophisticated harmonic balance program such as Agilent's ADS or Microwave Office from Applied Wave Research. Advancement in this area would probably result in much more progress, in terms of multiplier output power and efficiency, compared to other suggestions here at the cost of the most time and labour.

Further study into sputtered tungsten anodes could lead to improvements in diode performance that could rival or exceed the performance of diodes made with evaporated refractory metals. Ideality factors as low as 1.08 were achieved with annealed tungsten anodes at a very early stage in this work. It is this author's belief that a reduction in the series resistance of sputtered tungsten diodes could be achieved. Using thicker gold capping layers and a more in-depth study of sputtering power and annealing time, exploration of tungsten diodes would be a sensible investment of time.

9.5.2 New Projects

An attractive element to the design of this multiplier is the potential for scaling. Multipliers with higher or lower frequency outputs could be designed using the structure of the 200 GHz multiplier as a scalable reference. Not all elements of the multiplier could be scaled and optimising would be needed for values such as diode anode area and effective backshort position. However, it would be possible to implement, for example, the design for a 400 GHz multiplier from the structure developed in this work. A new photo mask would be needed with smaller diodes and modified filter patterns but the multiplier block would be effectively scaled to 50 %.

A new branch of integrated systems could include the combining of components, such as mixers and multipliers, on a single wafer chip. The objective of this would be to integrate a source, multiplier and mixer on a single chip potentially reducing RF losses between components. Costs would also be lower in recognition of instantly eliminating the need for two expensive milled component blocks.

Chapter 9 – References

[9.1] S. Martin, *et al.*, "Fabrication of 200 to 2700 GHz multiplier devices using GaAs and metal membranes," *IEEE MTT-S Digest*, vol. TH2D-2, 2001, pp. 1641-1644.

[9.2] C-I. Lin, *et al.*, "Planar Schottky diodes for submillimeter wave applications," *Terahertz Electronics Proceedings*, IEEE Sixth International Conference, 3-4 September 1998, pp. 135-138.

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A Suspended-Membrane Balanced Frequency Doubler to 200 GHz

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Abstract

A 200 GHz fixed tuned balanced frequency doubler using suspended membrane technology and integrated diodes is described. The design is discussed with reference to DC and RF circuit losses, integrated diode-membrane structure and ease of construction. Finite element analysis and harmonic balance methods were used to optimise multiplier performance. Predictions show peak power output of 15 mW and peak efficiency of 12 % at 200 GHz. Key device fabrication steps are also described.

Introduction

Radio astronomers have been utilizing heterodyne receivers for the mm and sub-mm wavelength region of the EM spectrum for over 30 years, the first successful observation being about 60 years ago [1]. Interstellar matter generally emits radiation in this band and through its detection a better understanding of its composition has been established. Heterodyne receivers have been used to monitor the global environmental conditions of the earth. Frequency multipliers are needed to produce the continuous wave (CW) local oscillator (LO) signal required for mixer operation. Multipliers with integrated diodes on membrane structures, first introduced by JPL [2], offer potentially higher efficiencies than conventional flip-chip bonded designs.

Multiplier Design

The multiplier mount is a planar crossed-waveguide design with a suspended microstrip cavity connecting the WR10 and WR5 guides (Fig. 1). A pair of Schottky varactor diodes are situated across the input waveguide in a balanced anti-series configuration at a distance L_{eff} from the suspended microstrip cavity. The varactors are grounded to the waveguide walls and a 9 element low pass filter provides the DC connection to bias the diodes while providing RF isolation at all other frequencies present. A fixed position output backshort provides optimum impedance matching between the quasi-microstrip transmission line (effectively an antenna spanning the output waveguide) and the reduced height output waveguide. The entire substrate is thinned down to ~ 20–30 um membrane to reduce dielectric losses.

This design is a development of work carried out by Porterfield [3]. The input waveguide is reduced in height so that the TM_{11} mode is not supported which is the lowest mode that can couple to the input waveguide at the output frequency. By doing this, currents produced in the diodes at the output frequency are restricted to the output circuit. The balanced anti-series design suppresses odd harmonics and eliminates the need for a lossy inter-waveguide distributed filter.

The waveguide mount is a split block design, each half milled with a precision CNC mill. Construction is very simple; the membrane chip can simply be dropped into the cavity and the relevant wire bond connection made. This has distinct advantages over flip-chip bonding including ease of integration into the mount and reduced series resistance.

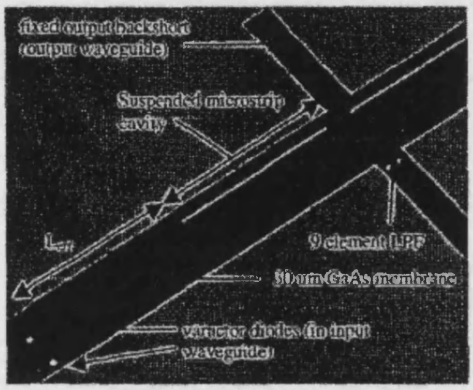

Fig. 1: 100/200 GHz frequency doubler showing lower half of split block and 30 um GaAs membrane

Optimization Process

The above structure was analysed using finite element analysis (Ansoft HFSS) and the embedding impedances determined at key frequencies for a range of values for L_{eff} (the effective backshort position as seen by the diodes). A harmonic balance method was used to derive diode efficiency and output power. The harmonic balance program was a customised program based upon the original written by Siegel and Kerr [4]. Efficiency and output power are at a maximum when L_{eff} = 0.97 mm. This is when the peak E-field is approximately a quarter of the guided wavelength from the terminating wall.

Expected performance was also computed as a function of epilayer doping concentration and of anode diameter (Fig. 2). Larger diodes can handle more power but have a larger zero bias capacitance which either requires a large reverse bias (and hence reverse breakdown on the diode) and/or high input power which may not be available. Small area diodes can saturate easily and may punch-through making ineffective

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multiplier devices. A varactor diode diameter of 13 um and doping density of $1x10^{17}$ cm^{-3} gave optimum predicted performance.

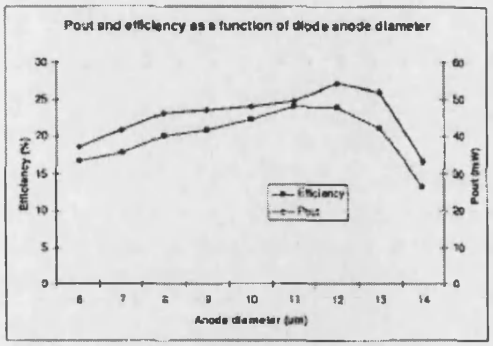

Fig. 2: Predicted P_{out} and efficiency at 200 GHz as a function of diode anode diameter

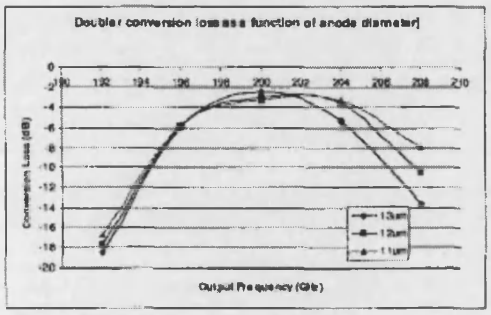

Fig. 3: Predicted doubler conversion loss to 200 GHz in a single diode

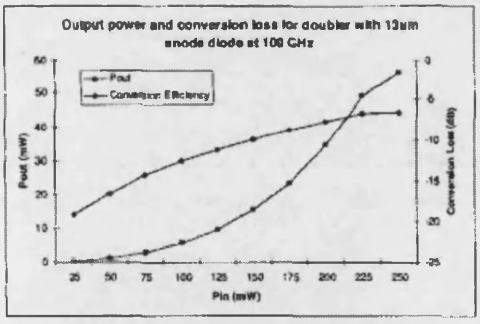

Fig. 4: Predicted P_{out} and conversion loss as a function of P_{in}

To reduce the parasitic capacitance, the planar diode employed has an air-bridged finger connecting the anode to a contact pad. The optimum values of finger width and length were found to be 4 µm and 50 µm, respectively. For the final optimised design, the multiplier conversion loss was determined as a function of frequency, with bias voltage and input power being optimised at each frequency (Fig. 3). Note, this is conversion loss in the diode and losses due to the mount (~ 2 dB) have not been included. Fig. 4 Shows the relationship between input power, output power and efficiency. It is expected that efficiency will start to drop when the diodes start to hit their saturation which will be around 75 – 100 mW and as a result maximum output power would fall short of expected.

Fabrication

All the fabrication processing steps required to make complete membrane devices have been developed. The ohmic contacts and varactor diodes are formed in the conventional photolithographic manner. Anode metallisation, anode contact fingers, transmission lines and filters are then deposited onto the chip. Reactive ion etching (RIE) is then performed to release the devices from the highly conductive n^+ layer in the GaAs wafer. The chip is than lapped down backside to 75 – 100 um. RIE is used again to perform a deeper (25 – 30 um) trench etch around the devices giving the slight 'T' profile. The chip is then front side mounted and back wet etched using sulphuric acid and hydrogen peroxide to realize the membrane. Chips are fragile but can be handled in tweezers with care.

DC testing of diodes has shown promising values of ideality, series resistance and reverse bias breakdown. Fig. 5 shows partially completed processing of the multiplier chip. Varactor diodes are situated on the LHS of the chip being connected to a 9-element low pass filter via a 20um wide transmission line. Test diodes and alignment marks make up the rest of the features.

Fig. 5: Photograph of 3 multiplier circuits before being etched into 'T' profile ready for mounting

Conclusions

A 200 GHz fixed tuned balanced frequency doubler using suspended membrane technology has been designed and optimised. Complete device structures are now being fabricated and RF measurements will follow shortly.

References

[1] R. Blundell, *et al.*, "Submillimeter receivers for radio astronomy", *Proc. IEEE*, vol. 80, Issue. 11, Nov. 1992 pp. 1702-1720.

[2] P. H. Siegel, *et al.*, "2.5-THz GaAs monolithic membrane-diode mixer", *IEEE Trans. On Microwave Theory and Techniques*, vol. 47, no. 5, May 1999, pp. 596-604.

[3] D. W. Porterfield, *et al.*, "A high-power fixed-tuned millimeter-wave balanced frequency doubler", *IEEE Trans. On Microwave Theory and Techniques*, vol. 47, no. 4, April 1999, pp. 419-425.

[4] P. Siegel *et al.*, "Topics in the optimization of millimeter-wave mixers," *NASA Technical Paper*, 2287, 1984.

A Membrane Planar Diode for 200 GHz Mixing Applications

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Abstract

The design and fabrication of a monolithically integrated subharmonic mixer for 200 GHz is described. The 1.5 μm diameter Schottky diodes are formed on a 5 micron thick GaAs membrane suspended across the RF waveguide. Predicted mixer performance shows improved conversion loss compared with that of conventional flip-chip diodes.

Introduction

The development of low-loss, heterodyne detection systems operating at teraheitz frequencies is essential for applications including atmospheric remote sensing and molecular line radio astronomy. Such applications need good quality air-bridged Schottky diodes for use in heterodyne mixers and frequency multipliers. A typical device consists of an anti-parallel pair of Pt/Au Schottky diodes, fabricated on GaAs [1]. Anodes are formed through via holes lithographically defined in a thin layer of SiO_2 covering the GaAs. Thick gold contact pads are deposited on top of the SiO_2, with narrow contact fingers connecting the anodes. An air-bridge etch is used to reduce parasitic losses by removing GaAs, with its high dielectric constant, from around the planar contact fingers (Figure 1).

At these frequencies, it is customary to dice and lap the devices, then to flip-chip solder them onto gold-on-quartz filter circuits for insertion into waveguide mounting structures. In the approach described here, the diodes are formed monolithically with a supporting GaAs membrane, eliminating the need for flip-chip soldering of devices.

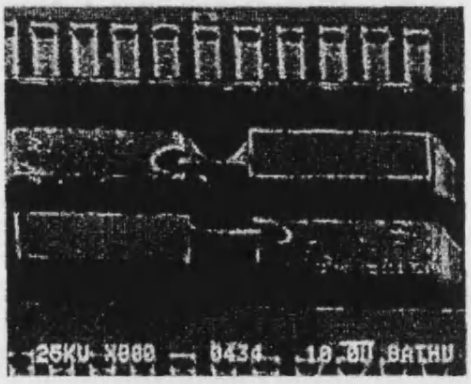

Fig. 1: Anti-parallel pair of air-bridged Schottky diodes, suitable for flip-chip mounting.

Mixer Design

In this subharmonic mixer design, the non-linearity of the diode is used to generate currents at twice the LO frequency, that mix with the RF signal. An anti-parallel diode configuration is used to suppress mixing with odd harmonics of the LO frequency (including fundamental mixing).

A sub-harmonic mixer has several attractive features. The signal and LO frequencies are well separated and can be isolated by simple filters within the mixer, thus avoiding the requirement for a low loss LO injection network. A simpler LO configuration can be used since power need only be generated at half the signal frequency. Broad, well matched instantaneous IF bandwidths can readily be achieved.

Although subharmonic mixers generally show higher noise temperature and conversion loss compared to fundamentally pumped waveguide mixers, the subharmonically pumped mixer is usually the preferred option for remote sensing applications because of the advantages described above.

The mixer mount uses a traditional, split-block crossed-waveguide configuration [2], the LO waveguide (WR-10) being perpendicular to the signal waveguide (WR-5). Both LO and signal waveguides incorporate reduced-height transformers to improve impedance matching. The waveguides are electrically coupled via an enclosed microstrip circuit. The microstrip circuit consists of filters to provide LO, signal and IF isolation. The diode pair is suspended across the centre of the signal waveguide in the E-plane direction. A bandpass filter connects the diode pair to a waveguide probe which protrudes into the LO waveguide and couples LO power into the diodes. The IF signal is coupled out through a low pass filter situated on the opposite side of the diode chip to the LO bandpass filter. A DC/IF return for the diodes is provided by a shorting wire connected to the microstrip line on the LO side of the circuit. Adjustable tuning backshorts are used in both signal and LO waveguides.

Conventionally, the filter metallisation is carried on a quartz substrate, typically of thickness ~ 75 μm. The GaAs device substrate is thinned to typically ~ 20 μm and the diodes flip-chip soldered onto the filter metallisation. The large amount of dielectric material surrounding the diodes adds significantly to the parasitic capacitance of the structure.

Figure 2 shows a schematic diagram illustrating the layout of the mixer diodes for the work described here. The anti-parallel diode pair, plus associated filter metallisation are supported by a thin substrate (~ 25μm) that is suspended in a channel

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machined across the RF input waveguide. In the region immediately surrounding the diode pair, the substrate is reduced to a thickness of ~ 5μm to reduce the parasitic losses.

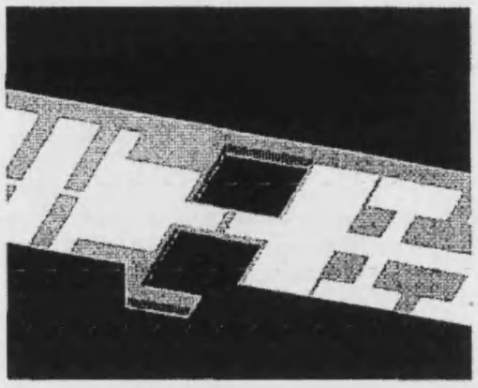

Fig. 2: Schematic illustrating membrane mixer configuration.

The above structure was analysed using finite element analysis (Ansoft HFSS) to determine the embedding impedances at harmonics of the LO and at the harmonic sidebands for a range of backshort positions. A harmonic balance method was used to derive conversion efficiency and mixer noise temperature. The harmonic balance program was a customised program based upon the original written by Siegel and Kerr [3]. For the purposes of comparison, a similar structure was modelled in which the membrane diode configuration was replaced by a structure representing a conventional flip-chip diode.

Figure 3 shows a comparison of the mixer conversion loss predicted for both flip-chip and membrane diodes, mounted in the same embedding structure. All the simulations were carried out for fixed positions of the tuning backshorts in both the LO and signal waveguides. The positions of the two backshorts were chosen to optimise the performance at 200 GHz. The plots thus indicate the instantaneous RF bandwidths available. The predictions clearly show the improved noise performance of the membrane devices.

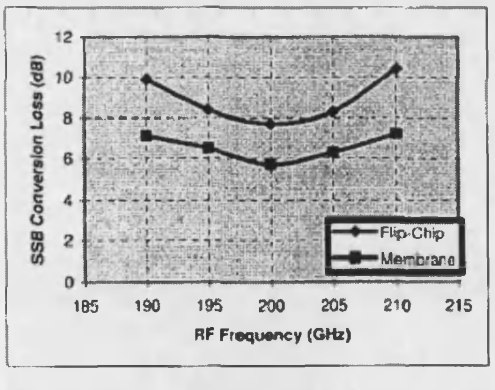

Fig. 3: Predicted conversion losses of flip-chip and membrane diodes in the same embedding structure.

Device Fabrication

All the processing steps necessary to fabricate membrane diodes have been successfully developed. Complete device structures are now being fabricated.

A combination of plasma and chemical etching is used to open up via holes in the SiO_2 layer, through which the Ti/Pt/Au anodes are deposited. The microstrip/bias circuit connected to the planar diodes is formed simultaneously with the device contact fingers. The gold metallisation is covered with a layer of chromium or titanium, to act as a protective mask during the plasma etch process that follows. The plasma etch is made to a depth of 5 μm and is used to remove the unwanted buried ohmic layer to isolate the diode contact pads. Figure 4 shows a device following this isolation etch process.

Following a lithographic patterning stage, a much deeper (~ 25 μm) plasma etch is made to define the ultimate depth of the GaAs supporting frame. The filter metallisation sits on top of a GaAs mesa that has a height of 25 μm. The GaAs sample is now mounted face down on a carrier wafer and the bulk GaAs substrate is removed by a combination of lapping and etching until the 25 μm thick mesa is freed from the bulk substrate.

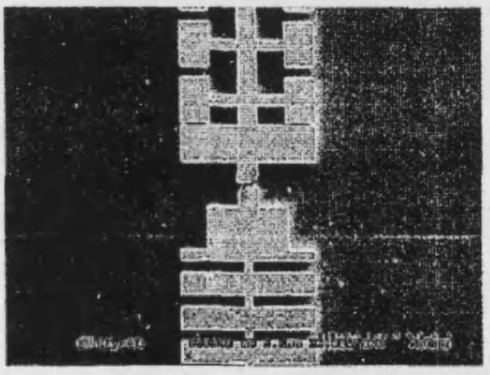

Fig. 4: Membrane diode structure following isolation etch and prior to formation of the membrane.

Conclusions

A membrane-supported planar Schottky diode has been developed for use in a subharmonically-pumped mixer designed to operate at a frequency of 200 GHz. Complete device structures are now being fabricated and RF measurements will follow shortly. Computational modelling predicts that a membrane device will operate with a conversion loss roughly 2dB lower than that expected from a conventional flip-chip diode.

References

[1] T. Crowe *et al.*, "GaAs Schottky diodes for THz applications", *Proc. IEEE* **80**, pp. 1827-1841 (1992).

[2] A.R. Kerr, "Noise and loss in balanced and subharmonically pumped mixers: Part 1 - Theory", *IEEE MTT*-27, pp. 938-943 (1979).

[3] P. Siegel *et al.*, "Topics in the optimization of millimeter-wave mixers," *NASA Technical Paper*, 2287 (1984).